Design and Optimization of Microwave Circuits and Systems Using Artificial Intelligence Techniques

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Design and Optimization of Microwave Circuits and Systems Using Artificial Intelligence Techniques

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To my brother and mother for their love and support

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SUMMARY

The evolutionary developments in wireless and mobile technology require complex device, circuit and package design. The modern microwave systems require improved computer aided design (CAD) techniques for accurate modeling, analysis and design. The current design methods are either simplistic and lack accuracy or are too complex to design and optimize. The work of this thesis was focused to develop CAD tools and methodologies that would provide greater accuracy and consume less time while providing the ability to handle large number of design variables. The proposed methodology should provide modeling, analysis and synthesis capability. It should be able to account for manufacturing variations and ensure high yield prior to high volume commercial fabrication. This research focused on developing artificial intelligence techniques like neural networks and genetic algorithms for microwave design.

In this thesis, a new combined neural network and genetic algorithm based approach called the neuro-genetic methodology is presented. In this method an accurate neural network model is developed from the experimental data. This neural network model is used to perform sensitivity analysis and derive response surface to obtain insight on trends and impact of design or layout parameters on electrical performance. An innovative technique is then applied in which genetic algorithm is coupled with the neural network model to assist in synthesis and optimization. The proposed method is used for modeling and analysis of circuit parameters of flip chip interconnects up to 35 GHz. The proposed method is also used for design of multilayer inductors and capacitors at 1.9 GHz and 2.4 GHz applications. The method was also used for synthesis of mm wave low pass filters in the range of 40-60 GHz for desired electrical response. The

devices obtained from layout parameters predicted by the neuro-genetic design method yielded electrical response close (95% accuracy) to the desired value. The proposed method also implements a weighted priority scheme to account for tradeoffs in microwave design. This scheme was implemented to synthesize bandpass filters for 802.11a and HIPERLAN wireless LAN applications in the range of 5-6 GHz. The scheme did results in providing optimal design within given constraints.

This research also develops a novel neuro-genetic design centering methodology for yield enhancement and design for manufacturability of microwave devices and circuits. An accurate neural network model is used to calculate yield using Monte Carlo methods. A genetic algorithm is then used for yield optimization. The proposed method has been used for yield enhancement of SiGe heterojunction bipolar transistor and mm wave voltage-controlled oscillator. It results in significant yield enhancement of the SiGe HBTs (from 25 % to 75 %) and VCOs (from 8 % to 85 %). The proposed method is can be extended for device, circuit, package and system level co-design since it can handle a large number of design variables without any assumptions about the component behavior.

The neural network and genetic algorithm based methods developed in this thesis have speed and accuracy advantage over existing methods. They have been validated on various devices like flip chip interconnects, capacitors, inductors, mm wave filters, bandpass filters, SiGe HBTs and voltage-controlled oscillators. The proposed algorithm could be used by microwave community for design and optimization of microwave circuits and systems with greater accuracy while consuming less computational time.

CHAPTER 1

Introduction

The emergent use of wireless technology in numerous electronic systems to enhance portability, functionality, and compatibility has resulted in a rapid evolution of microwave design. System-on-package (SOP) and system-on-chip (SOC) design solutions, along with novel device topologies have been proposed to meet the demands of higher performance, miniaturization, and lower cost. These solutions require improved computer aided design (CAD) techniques. The goal of this research is to develop improved CAD techniques for design and optimization of microwave circuits and systems. This chapter discusses emerging trends in development of microwave devices and issues in modeling and design of microwave components, along with an overview of existing modeling and optimization methods. The chapter also discusses the motivation and objectives of this research and organization of this thesis.

1.1. Emerging Trends in Microwave Circuits and Components

The foundations of microwave engineering originated from fundamental concepts of electromagnetic theory formulated by James Clerk Maxwell more than 100 years ago [1]. Earlier applications of microwave circuits were limited to radar systems. Radar systems have been used for detecting and locating air, ground, or seagoing targets and for air-traffic control systems, missile tracking radars, automobile collision-avoidance systems, weather prediction, motion detectors, and a wide variety of remote sensing applications. The development of transistors in 1956 at Bell Laboratories led to further advances in

microwave engineering. Microwave technology is an important component of most consumer electronics products today. Most wireless telecommunications systems, such as direct broadcast satellite (DBS) television, personal communication systems (PCSs), wireless local area computer networks (WLANS), cellular phones, video (CV) systems, and global positioning satellite (GPS) systems, rely heavily on microwave technology. The design specifications for these different systems vary from application to application. Short range wireless systems for factory and indoor applications require Bluetooth™ and ZigBee™ standards [2]. These systems require robust performance despite the harsh electromagnetic environment inherent in industrial and indoor floors. Furthermore, they should operate on low power budgets to be economically viable. On the other hand, wireless LAN devices require higher frequencies and greater bandwidths to enable higher data rate. The microwave devices used in medical, military, and space application require protection from the harsh ambient environments in which they operate. The microwave components of handheld devices require compact size and low power consumption. There is increasing emphasis on multi-band and reconfigurable designs to enhance portability, compatibility and functionality of wireless devices due to various standards and emerging applications.

In order to meet the various demands of emerging applications, more complex device and packaging designs are used. To obtain higher frequencies of operation, transistors with smaller gate lengths and more exotic materials- like silicon germanium and compound semiconductors- are used. Novel transistor topologies - like heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs) -are used over traditional silicon bipolar and field effect transistors to obtain higher performance [3].

SOC designs are gaining popularity due to low cost and compact design. At the system level, there is higher level of integration of microwave components with digital, optical, analog and even MEMs devices. SOP design involving multilayer integrated passives has emerged as another popular solution to meet the increasing demands of miniaturization and cost [4]. These emerging solutions are increasing the complexity of microwave device and system design, giving rise to numerous design challenges.

1.2. Issues in Design of Microwave Components

The evolution of device topologies and packaging technologies has posed serious design challenges to microwave engineers. The design of a microwave circuit is comprised of two stages: 1) modeling and analysis, and 2) optimization and synthesis. Current design methods are too simplistic, lack accuracy and are too complex to derive and optimize. Most design strategies are limited to stage 1 and are not holistic. There is a need for an integrated design approach involving both stages of the design cycle.

The complex device topologies of heterojunction bipolar transistors and HEMTs require more efficient and accurate modeling methods. Low yield and high cost has limited the use of these devices over traditional silicon-based transistors, despite superior performance. Multilayer integrated passive technology implements passives in a configuration having a complex, three-dimensional geometry over various layers of different substrates. This leads to challenges in modeling inner-layer capacitive effects, dielectric losses, via effects, and substrate coupling. Design tools require high level of nonlinear modeling capabilities to model complex relationships between the design variables and performance specifications of these devices. High-frequency design at

millimeter wave (mm-wave) frequencies differs from low-frequency design in several aspects. There is enhanced parasitic coupling, enhanced transmission, and radiation loss. Furthermore, the effects of metal roughness and dielectric constant variations have significant impact on mm-wave circuit performance [5]. Electromagnetic simulation methods are inadequate for such circuits because they require approximation, either in the description of the structure to be analyzed (metal roughness and surrounding environment) or in terms of boundary conditions.

The second stage in microwave design is optimization and synthesis. Microwave circuit optimization is a multi-parameter problem in which several design requirements must be met simultaneously. Single parameter optimization may result in the failure to meet other design specifications. For example, during the design of a power amplifier, an improvement in amplification linearity could lead to lower power efficiency. In inductor design, an increase in quality factor may lead to a change in the desired inductance. Similarly, for a bandpass filter design, it is difficult to obtain narrow band, low insertion loss in the pass band, and high rejection in the cutoff region simultaneously. The optimization and synthesis method must incorporate trade-offs among design parameters to obtain best possible solution within given design constraints. The method must be application-specific, even for same type of device. The transistors used the power amplifiers would require high gain, linearity, and low power consumption, but those used in low-noise amplifiers would require a low noise figure.

The commercial use of the microwave devices requires high yield at reduced cost. There are always inherent fluctuations in circuit performance due to random manufacturing variations. For high-volume manufacturing, the optimization process must

account for variance. A method involving optimization of the mean value of design parameter only may lead to low yield design. The yield maximization problem is concerned with optimizing the number of fabricated circuits whose performance meets a set of desired specifications.

As technology moves to higher frequencies and greater levels of integration (along with compact design), the number and complexity of design variables is increasing. Microwave systems require optimization in a holistic fashion. This implies that the CAD tools must perform optimization on IC, package and board level parameters simultaneously. An IC design may not be optimal from the signal integrity or package or board level perspective. Therefore, the modern CAD tools must have an integrated design approach for circuit, package, and system level co-design to obtain an overall optimized system. This requires a powerful design methodology that can account for all design variables during pre-layout design.

1.3. Overview of Modeling and Optimization Methods

Current modeling techniques can be classified as follows: 1) statistical methods; 2) physical or analytical methods; 3) numerical methods; and 4) neural network methods. Each of the four methods has advantages and disadvantages. Statistical methods involve fitting regression equations relating layout parameters to electrical characteristics of devices. These methods are the simplest to implement and interpret, but are limited by range and accuracy. There is a serious tradeoff among the amount of experimental data available, complexity of the regression model, and accuracy of the model. Statistical methods are best suited to devices with linear or limited nonlinear characteristics and

simplistic design topologies. Analytical or physical models, on the other hand, can be difficult to derive for new devices. Most analytical models make assumptions regarding boundary conditions or device topologies to simplify models. This lowers the accuracy of the models. Numerical methods used by popular electromagnetic (EM) simulators provide sufficient accuracy, but are computationally extensive [6]. The results obtained from analytical and numerical methods vary from the measured data because process variations and other electrical characteristics cannot be modeled accurately.

Neural networks represent an efficient alternative to conventional methods, since they can be used to generate accurate models for existing and new devices directly from the measured data, thus accounting for manufacturing variations and parameter indeterminacy issues [7]. No assumptions about the component behavior are made when developing neural network models. Neural networks have been used extensively in modeling passive and active microwave circuits [8]. Although neural networks have superior performance in modeling nonlinear data, they do not possess great extrapolation capability. Their modeling accuracy is valid only in the range in which they have been trained. Therefore, the generation of training data generation requires careful planning to cover the design space effectively. Neural networks are used along with existing CAD methods to enhance accuracy and speed of microwave modeling and design [9-10].

The models obtained from the various modeling techniques can be used by microwave designers for analysis. Device analysis based on models enables the designers to obtain insight into the working of the device. It also provides information about the impact of design variables on the electrical response of the device. Most CAD methods

contain capabilities of correlation analysis, sensitivity analysis, statistical significance tests and response surface plotting for analysis and interpretation of data from the models.

To complete the microwave design cycle, the models obtained using various modeling methods are used for synthesis and optimization of devices with desired specifications. Optimization is an important step in the CAD process, as it converts an initial (and quite often unacceptable) design into an optimized final design meeting the given specifications. Unfortunately, this step can consume a large amount of time due to its iterative nature. Linear optimization methods such as the simplex and dual simplex methods require continuous variables with a single linear objective function and linear constraints [11]. Such methods are inadequate for optimizing complex microwave circuits and components involving nonlinear objective functions and solution spaces. Nonlinear optimization methods like the gradient descent approach and Newton's method have also been used extensively to optimize the performance of microwave devices [12]. Most nonlinear methods are suitable for single-parameter optimization. However, microwave circuits often require multi-parameter optimization to meet several design specifications simultaneously. Traditional optimization methods require continuity of design space, explicit objective function and derivative information of the optimization function. In practical microwave circuits such conditions are difficult to obtain. Moreover, traditional methods take a local view of optimization, where it is critical to find the good starting point and best search direction. This approach can lead to identifying a local optimal point rather than the global one. Genetic algorithms (GAs) have been used for design and optimization of microwave circuits such as filters because of their efficiency in nonlinear multi-parameter search and optimization [13]. GAs have

been used in conjunction with EM tools for circuit optimization [14]. However, the time-consuming nature of EM simulations limits the use of these tools for interactive optimization using genetic algorithms. GAs can sort out the overall optimal area very fast, but converging to a global optimum point is very slow. Some hybrid algorithms involving traditional optimization methods can be used to overcome this problem.

To ensure the design for manufacturability of microwave devices single point optimization without the variance component is inadequate. Microwave circuits also require design centering and yield optimization prior to high volume manufacturing to ensure low cost and manufacturability. This is required since during the manufacturing process, the design variables are not exact single point values specified by the designer. There have been several methods used for yield enhancement of specific microwave devices [15-17]. Most of the methods in the literature are either geometrical or Monte Carlo methods [18]. Monte Carlo methods are time-consuming and thus prohibitive for most microwave devices. Geometrical methods seek an indirect solution through the construction of an approximation to the acceptability region. These methods assume continuity and some convexity of space. They have limited ability to handle large number of design variables, as there is dramatic increase in complexity.

1.4. Research Motivation and Objectives

The design challenges due to evolutionary developments in microwave circuits and components provide tremendous opportunity to microwave community for research and development. The accurate and efficient design of microwave circuits and systems is still a topic of active research and open debate. The problem in modeling and optimization of

microwave circuits requires novel methodologies and more integrated strategies. Current design tools face limitations of accuracy, speed and the ability to handle complexity. Novel design methodologies are required to meet the requirements of evolving applications, greater performance, higher yield, and lower time to market, while maintaining lower cost.

The goal of this research is to develop methodologies to meet the design challenges of modern microwave devices. This research involves: 1) the development of a design and optimization methodology for complex microwave devices and circuits; 2) a feasibility study and application of the proposed methodology on passive devices; 3) the development of a novel design centering and yield enhancement methodology for design for manufacturability; 4) an application of the proposed methodology on microwave devices like heterojunction transistors; and 5) the proposal of an integrated design methodology for circuit, package, and system level co-design.

1.5. Thesis Organization

The remainder of this thesis describes the neural network and genetic algorithms based methodology for design and optimization of microwave circuits and systems. It also identifies the application and provides results of the proposed methodology on various microwave circuits and components. Chapter 2 provides discussion on neural networks and genetic algorithms. It also presents the proposed neuro-genetic methodology for design of microwave circuits. Chapter 3 describes the application of neural networks for modeling and analysis of flip chip interconnects. In Chapter 4, the proposed neuro-genetic methodology is used for design and optimization of multilayer

inductors and capacitors. Chapter 5 demonstrates the results of microwave filter synthesis using neuro-genetic algorithms. The method is used for synthesis of mmWave low pass and 802.11 band pass filters.

A novel neuro-genetic design centering and yield enhancement methodology is presented in Chapter 6. In this chapter, the methodology is used for design centering of silicon germanium (SiGe) heterojunction bipolar transistors. This chapter also describes how this method can be used for an integrated circuit, package, and system level co-design and its application for a voltage-controlled oscillator design. Finally Chapter 7 summarizes main contributions of this thesis and lists possible future research directions.

CHAPTER 2

Artificial Intelligence Techniques

Artificial intelligence techniques have gained popularity in engineering design in recent years due to their efficiency and effectiveness [19]. Artificial neural networks have emerged as a powerful technique for modeling general input/output relationships. Genetic algorithms are efficient in search and optimization. This chapter describes these methods. It also discusses their application for design of microwave circuits and systems.

2.1 Neural Network Modeling

A neural network has at least two physical components, namely, the processing elements and the connections between them. The processing elements are called neurons, and the connections between neurons are known as links. Every link has a weight parameter associated with it. Each neuron receives stimuli from neighboring neurons connected to it, processes the information, and produces an output. Neurons that receive stimuli from outside the network are called input neurons. Neurons whose outputs are used externally are called output neurons. The remaining neurons within the network are called the hidden neurons. There are different ways in which information can be processed by a neuron, and different ways of connecting them. There are several neural network structures and algorithms including multilayer perceptions (MLP) [20], radial bases function networks (RBF) [21], wavelet neural networks [22], self-organizing maps

[23], and recurrent networks [24] that have been used for microwave modeling and design [25].

Multilayer perceptrons (MLP) are the most popular type of network that falls to a general class of structures called feedforward neural networks. They are capable of approximating generic classes of functions, including continuous and integrable functions [26]. The structure of an MLP (Figure 1) is well-established, and the model has good generalization capability. The network consists of one input layer, one output layer and one or more hidden layers.

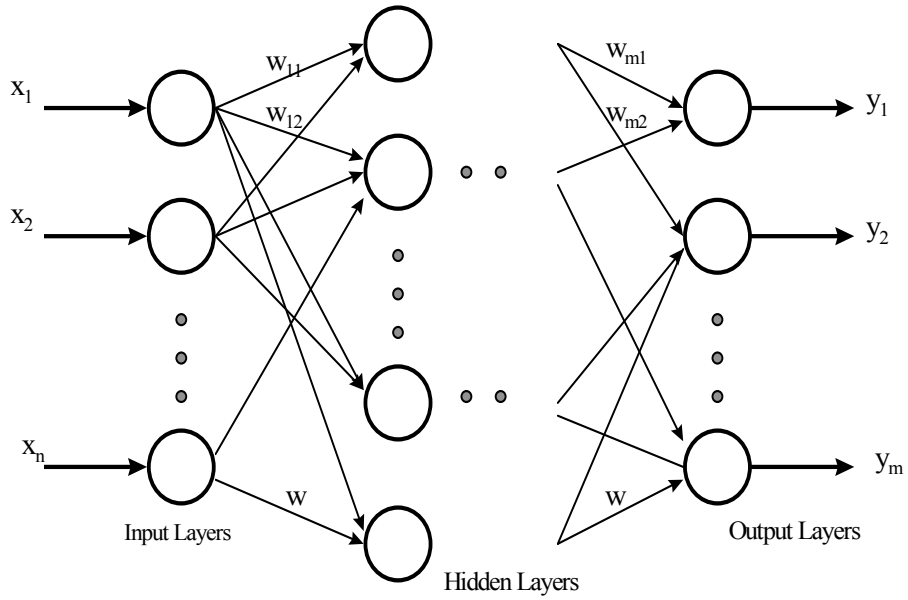


Figure 1: Multilayer perceptrons (MLP) structure

In a neural network, each neuron (except input layer neurons) receives the process stimuli (inputs) from other neurons. The weighted inputs to a neuron are accumulated and then passed through an activation function, which determines the neuron's response. A commonly used activation function, the hyperbolic-tangent is given by:

$$\sigma(\gamma) = \frac{(e^{\gamma} - e^{\gamma})}{(e^{\gamma} - e^{\gamma})} \tag{1}$$

Training a neural network involves updating the weights in such a manner that the error between the outputs of the neural networks and the actual response being modeled is minimized. A popular method of network training is the error back-propagation (BP) algorithm [27]. BP is a supervised learning method that uses gradient descent, which systematically changes the network weights by an amount proportional to the partial derivative of the accumulated error function, *E*, with respect to given weight [28]. The weight change is given by:

$$\Delta w_{ijk} = -\eta \frac{\partial E}{\partial w_{ijk}} \tag{2}$$

where *i* denotes a node in layer *k*, *j* is a node in the preceding layer *(k-1)*, and w_{ijk} is the weight between these two nodes. The constant η (which lies in the range 0-1) is called the learning rate. The learning rate determines the speed of convergence by regulating the size of weight changes. A larger rate may result in the algorithm settling at a local minimum. A smaller rate can promote stability, but results in longer training time. In order to improve training, an additional momentum term can be added. The momentum term deters the algorithm from settling in local minima and increases the speed of convergence. The weight of the back propagation at the $(n+1)^{th}$ iteration is then given by:

$$w_{ijk}(n+1) = w_{ijk}(n) + \eta \Delta w_{ijk}(n) + \alpha \Delta w_{ijk}(n-1) \tag{3}$$

where α (also in the 0-1 range) is the momentum constant.

The performance of the network is evaluated in the terms of its training and prediction errors. Each measure of learning capability is quantified by the root-mean-squared error (RMSE), given by:

$$RMSE = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}\left(y_i - \hat{y}_i\right)^2} \tag{4}$$

where n is the number of trials and y_i is the measured values of each response, and $\hat{y}_i$ is the neural model output. The training error is the RMSE of the data used for network training, and the prediction error is the RMSE of the data reserved for network testing. Network structure and training issues, such as the number of layers, number of neurons, the learning rate and the momentum constant are determined during the model development process. These values are selected so that after training, the network model outputs best match the experimental data.

2.2 Genetic Algorithms

A genetic algorithm is a guided stochastic search technique based on the mechanics of evolution and natural selection [29]. GAs typically operate through a simple cycle of four stages: (1) the creation of a "population" of a strings, (2) the evaluation of each string, (3) the selection of "most-fit" string, and (4) genetic manipulation to create a new population. In each computational cycle, a new generation of possible solutions for a given problem is produced. At the first stage, an initial population of randomly generated potential solutions is created as a starting point for the search process. Each element of the population is encoded into a string (the "chromosome") to be manipulated by genetic operators. In the next step, the performance (or "fitness") of each individual of the population is evaluated with respect to constraints imposed by the problem. Based on each individual string's fitness, a selection mechanism chooses "mates" for the genetic manipulation process. The selection policy is responsible for assuring survival of the most "fit" individuals.

Chromosome specification requires encoding each variable into a binary string,

although alphanumeric strings can be used as well. One successful method of for coding multi-parameter optimization problems is concatenated, multi-parameter, mapped, fixed-point coding [30]. If $\alpha \in [0,2^l]$ is the parameter of interest (where l is the number of bits in the string), the decoded unsigned integer α is mapped linearly from $[0,2^l]$ to a specified interval $[U_{min}, U_{max}]$. In this way, both the range and precision of decision variables can be controlled. The precision (π) of the mapped coding may be calculated as:

$$\pi = \frac{U_{\max} - U_{\min}}{2^l - 1} \tag{5}$$

The multi-parameter code is constructed by concatenating as many individual parameter strings as required. Each bit string may have its own sub-length or range. Figure 2 illustrates 2-paramater coding where the ranges of the first and second parameters are 1-8 and 0-31, respectively.

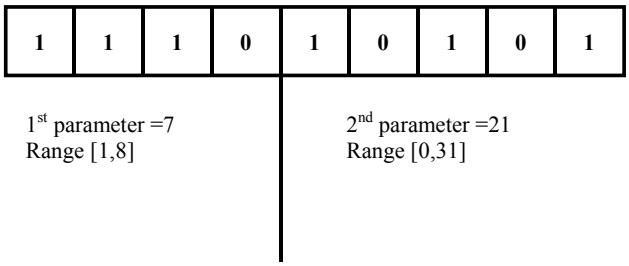


Figure 2: Multi-parameter coding.

Genetic operators (reproduction, crossover, and mutation) are used to create a new population of "offspring" by manipulating the genetic code of members ("parents") of the current population. Reproduction is the process by which strings with high fitness values (i.e., good solutions to the optimization problem under consideration) are selected to have large number of copies in new population. This process is based on a probabilistic method called *elitist roulette wheel selection*, where chromosomes with large fitness values are assigned a proportionately higher probability of survival into the next

generation. The probability of selection is given by:

$$P_{select\_i} = \frac{F_i}{\sum F} \tag{6}$$

The constraints imposed by the optimization problem determine that value of fitness function (F), which is given by:

$$F = \frac{1}{1 + \sum_n \left| K_n (y_d - y_o) \right|} \tag{7}$$

where n is the number of response variables, K_n are the weights of the responses, y_d represent the desired response and y_o are the outputs that result from the current input parameters.

After reproduction, the chromosomes that have survived are stored in a “mating pool" and await mutation and crossover operations. The crossover operation takes two parents and interchange part of their genetic code to produce two new chromosomes. The mutation operation is implemented by randomly changing a fixed number of bits every generation based on a specific mutation probability. The mutation operation is needed to account for the possibility that the initial population may not contain all of the genetic information needed to solve the problem.

Typical values for the probabilities of crossover and bit mutation range from 0.60 to 0.95 and 0.001 to 0.01, respectively. Higher mutation and crossover rates disrupt good “building blocks” more often, and for smaller populations, sampling errors tend to wash out the predictions. For this reason, the greater the mutation and crossover rates and the smaller the population size, the less frequently predicted solutions are confirmed.

2.3 Neuro-Genetic Design

The neural networks are fast and accurate method for modeling microwave devices. Previous work on the application of neural networks for microwave modeling has focused primarily on obtaining models relating layout parameters to electrical characteristics. There have been attempts to extend neural network models for synthesis and optimization [31]. However, such methods have been limited to extrapolation of the models to optimize a single layout parameter using the gradient descent approach [32]. This approach is not suitable for multivariable microwave optimization. There have been other methods used to optimize layout parameters by implementing neural networks as reverse functions to model layout parameters as outputs and performance parameter as inputs [33]. However, such a method may yield layout parameters that may not be feasible or out of range for fabrication. Also, this method cannot implement a priority scheme when several tradeoffs among design parameters are involved in optimization.

Genetic algorithms (GAs) have been used for the design and optimization of microwave circuits (such as filters) because of their efficiency in nonlinear search and optimization [34-35]. The genetic optimization method uses successive iterations to obtain the desired optimal point. Neural networks accurately map nonlinear relationships, and genetic algorithms are efficient in nonlinear multi-parameter search. This thesis combines the two approaches to obtain a novel neuro-genetic design methodology [36-37]. The proposed methodology has two stages. In the first stage, a neural network model is developed from experimental data. This model can be used to perform sensitivity analysis and obtain response surfaces. The next stage involves coupling the neural network model with genetic algorithms for subsequent design synthesis and optimization. This stage is the original contribution of this research and, to the best of the author's

knowledge, has not been reported previously. This methodology has the following salient features:

1) Generates neural network models directly from measured data, thus accounting for manufacturing variations;

2) Uses these models to perform sensitivity analysis and obtain response surfaces;

3) Performs multi-parameter optimization and synthesis using a priority scheme to account for various tradeoffs;

4) Consumes significantly less computational time as compared to EM simulation methods.

2.3.1. Stage 1: Neural Network Modeling and Analysis

Consider the example of a microwave device or component. The physical/layout parameters of the device determine the electrical characteristics. The inputs and outputs of the corresponding neural network model to encode the element's input/output relationship can be represented by

$$x = [L \;\; W \;\; H .... f]^T \tag{8}$$

$$y = [S_{11} \;\; S_{12} \;\; Q \;\; C .....]^T \tag{9}$$

where *L, W,* and *H* are layout parameters of the device, and *f* is frequency. The S_{ij} matrix elements denote the S-parameters of device, and Q and C are other electrical characteristics of passive device. For inductors and capacitors, these may represent quality factor, self-resonant frequency, or lumped component values (i.e., inductance and capacitances). For microwave filters, they could be bandwidth, cutoff frequency, center frequency, or insertion loss. The objective of neural network modeling is to find a

functional relationship between y (electrical characteristics) and x (layout or physical parameters). The neural network requires training using experimental data to map the functional relationship. In this section, we describe the important steps and issues in model development and performing analysis using the models to extract important information about the circuit behavior.

2.3.1.1 Problem Formulation and EM Simulations

The first step in model development is the identification of inputs and outputs. The inputs are generally the layout or geometrical parameters, and the outputs are the electrical responses of the microwave component. For example, insertion loss, return loss, and bandwidth are reasonable responses for passive filters. Similarly, quality factor, self-resonant frequency, and inductance values are typical responses for inductors. If there are several input parameters to investigate, a screening experiment can be performed to eliminate any statistically insignificant parameters. Initial EM simulations can be performed to characterize the layout parameters and performance parameters. The initial simulations provide the approximate behavior of microwave components. These results can be used to determine the range and magnitude of layout parameters that give a crude estimate of the range of electrical response and whether they fall within targeted specifications.

2.3.1.2 Experimental Design

This step is used to determine the exact range of data to be used for neural network model training. The results obtained from EM simulations can be used to determine this. If the range of input space ($\boldsymbol{x}$ space) in which the neural model would be used after training is $[\boldsymbol{x}_{min}, \boldsymbol{x}_{max}]$, then training data is explored slightly beyond this range (i.e.,

[$\boldsymbol{x}_{min}-\delta$, $\boldsymbol{x}_{max}+\delta$], where δ is a small increment in the parameter in question). This is done to ensure reliability of the neural model at the boundaries of model utilization range. Test data is generated in the range [$\boldsymbol{x}_{min}$, $\boldsymbol{x}_{max}$].

Once the range of input parameters is finalized, an experimental design is determined to obtain maximum information with a minimum number of experimental runs. This can be done using various sampling distributions, including uniform grids, non-uniform grids, statistically designed experiments [38], star distributions [39], and random distributions. In a uniform grid distribution, each parameter is sampled at equal intervals. In a non-uniform grid distribution, parameters are sampled at unequal intervals, which is useful when the problem behavior is nonlinear in certain sub-regions of the $\boldsymbol{x}$ space and denser sampling is required. Sample distributions based on designed experiments (such as factorial designs or central composite designs) and star distributions are used when the training data generation is expensive. There is another stratified sampling technique, called Latin hypercube sampling (LHS), where random variables are divided into equal probability distributions [40]. This is a technique whose performance and methodology lies somewhere between to that of designed experiments and *Monte Carlo* simulations.

2.3.1.3 Data Acquisition

Once the ranges and sampling distribution for the layout parameters are determined, the samples are simulated using an EM simulator or fabricated. EM simulator is used to extract the electrical characteristics of the device. The fabricated samples are measured using an RF/microwave measurement set-up (typically, S-parameter measurements from a network analyzer). The measurement data is used to extract the electrical characteristics of the device.

2.3.1.4 Neural Network Model Development

The experimental data is used to train a neural network. Training is accomplished using the BP algorithm. The layout parameters are the inputs to the neural network, and the electrical responses are the outputs. The other network parameters (i.e., number of hidden layer neurons, learning rate, and momentum constant) are chosen to optimize accuracy and speed of convergence of the neural network model. The accuracy of the neural network is determined during the testing stage. Testing is done using data samples that have not been used during training. Generally 75% of the available data is used for training and 25 % for testing. The RMS error is calculated using (4). A training error less than 5% is generally considered acceptable.

2.3.1.5 Sensitivity Analysis and Response Surfaces

Sensitivity analysis can be performed based on the neural network model to quantify the variation in an output response for an incremental change in a particular input parameter. The sensitivity of one output value is found by computing the partial derivative of the response with respect to the input of interest while holding the others constant [41]. This is represented by the relationship:

$$\frac{df}{dx_i} \cong \left. \frac{f(x + \Delta x_i) - f(x)}{\Delta x_i} \right|_{\Delta x_i \to 0} \tag{10}$$

where f is the functional relationship encoded in the neural network model, x is vector of layout parameters, and Δx_i is an incremental change in one of the elements of x. In this application, sensitivity analysis determines the magnitude of the impact of each layout parameter on the electrical response of the circuit. The results of sensitivity analysis are valid at a particular point. Response surface plots, however, can reveal overall trends. To

graphically illustrate trends in the variation of electrical along the range of layout parameters studied, 3-D response surface plots can be generated from the neural network models. A flow chart for the first stage of the approach is shown in Figure 3.

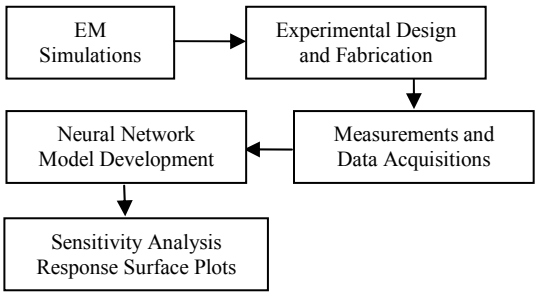


Figure 3. Stage 1: Neural network modeling and analysis.

2.3.2. Stage 2: Genetic Algorithm Optimization and Synthesis

The neural network model developed in stage 1 is used for design and optimization of microwave devices using genetic algorithms in stage 2. The desired electrical characteristics are provided to the genetic optimizer, which starts with an initial population of layout parameters. It then computes the response of this population using the neural network model and selects the best (i.e., most fit) samples and performs genetic manipulation to obtain results from the best samples. The process continues until the remaining samples produce the set of layout parameters that give (or are closest to) the desired electrical characteristics.

An advantage of the genetic approach is that it can assign priority to preferred performance characteristics (through the K_n's in (7)). For an inductor, in some cases the specific value of inductance is important, as it can alter the operation of circuits like matching networks and voltage controlled oscillators. On the other hand, some applications require a high quality factor, and the inductance may vary slightly. Similarly,

for filter design, various tradeoffs between electrical design parameters (like bandwidth and insertion loss) can be accounted for using priority assignment during genetic optimization. Due to this flexibility, the design procedure can be customized to suit a particular application. The flowchart for stage 2 is shown in Figure 4.

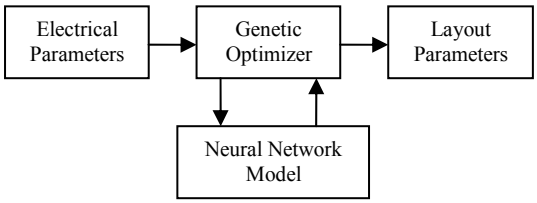


Figure 4. Stage 2: Neuro-genetic optimization and synthesis

2.4 Neuro-Genetic Design of Microwave Devices

Modern microwave design is accomplished using computer-aided design (CAD) tools based on numerical or analytical methods. Preliminary design involves determining layout approximations from analytical expressions derived from Maxwell's equations. Next, CAD tools are used iteratively for optimization and synthesis to obtain the set of layout parameters that meet desired electrical specifications. Samples with optimized layout parameters are then fabricated. There is often an appreciable difference in the measured electrical response of the fabricated devices from expected results because of manufacturing variations, parameter indeterminacy issues, and other nonlinearities not modeled by CAD tools. The layout parameters are thus revised, and more samples again fabricated until the desired electrical specifications are satisfied. A generic flow diagram of the design process is shown in Figure 5. The design flow process has two iterative loops. The first is within the CAD tool. Typically hundreds of iterations may occur in this loop to obtain an optimal design. Considering the computationally intensive nature of the

electromagnetic field solvers, this may take enormous computational time and memory resources, particularly for complex structures.

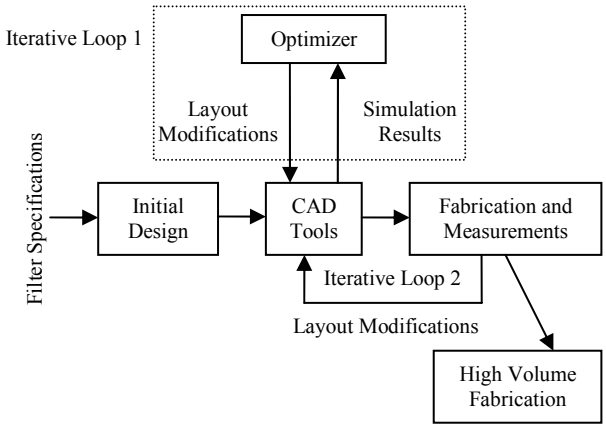


Figure 5. Microwave design process flow.

There is generally a second loop after fabrication due to performance shifts caused by manufacturing variations, invalid assumptions, and inaccuracies in the CAD simulations. This second loop consumes even more time and resources. The layout modifications in this loop are usually accomplished using a designer's experience (as opposed to a more systematic approach) because CAD tools are limited in their ability to use measured data for optimization. This thesis presents several examples in which a neuro-genetic design technique is used in the design loops to minimize the time and cost while providing sufficient accuracy. In one example, the proposed method is used in the CAD iterative loop. Three examples involving fabrication iterative loop are also presented.

CHAPTER 3

Modeling Flip Chip Interconnects

Flip chip interconnect technology provides higher packaging density (a greater number of I/Os), improved performance (shorter leads, lower inductance and better noise control), a smaller device footprint, a lower packaging profile, and lower cost. The electrical characteristics of interconnects affect the performance of high-frequency microwave circuits. Therefore, precise modeling and characterization of these interconnections as a function of layout parameters is important to optimize the performance of flip chip signal transitions, and ultimately, to enhance the performance of microwave circuits [42]. To enable design for manufacturability of microwave components, fast and accurate interconnect models are required. Very accurate models with physical/geometrical information that includes electromagnetic effects are needed for design and optimization. Statistical models have been used to model behavior of flip chip interconnections [43]. However, models using neural networks have been shown to exhibit superior performance in both accuracy and predictive capability over statistical techniques [44]. This chapter presents a neural network-based technique for modeling and analyzing the electrical performance of flip chip transitions up to 35 GHz [45].

3.1. Experimental Design

Flip chip technology has been analyzed electrically, mechanically, and thermally to determine its advantages and disadvantages [46]. There are several factors that affect the

electrical performance of flip chip transitions. These include transmission line type, dielectric constant of the mounting substrate, bump height, bump diameter, conductor overlap, bump misalignment, underfill type, and the number and position of multiple signal and ground bumps. However, only a few parameters have a significant impact on performance [47].

The flip chip devices under investigation were mounted on ceramic or organic substrates. The devices were first bumped with solder balls and then mounted (flipped) onto the substrate. A coplanar waveguide (CPW) structure was used as the transmission line for these experiments because of ease of fabrication and reduced mismatch, coupling, and resonance effects. There are several factors that affect the electrical behavior of the flip chip interconnection. Empirical analysis of the simple flip chip configuration shown in Figure 6 led to the selection of the following factors for experimental design and model development:

- *o* conductor overlap (bumps are always placed in the center of the overlap area);
- *w* CPW signal line width;
- *d* distance from ground bump center to the edge of the ground plane;
- *a* bump diameter; and
- *h* bump height.

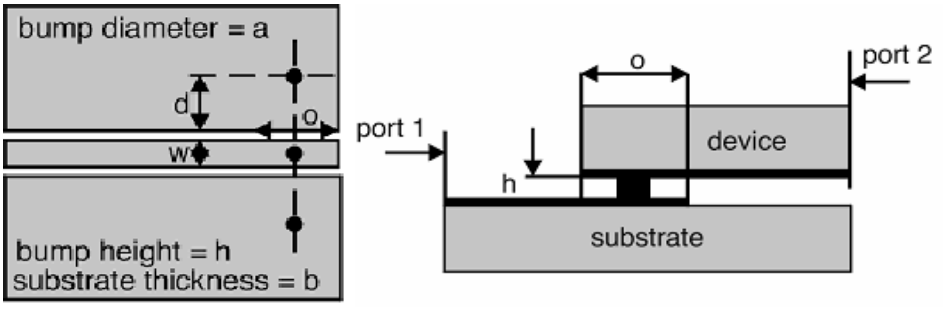


Figure 6. Schematic of bump configuration.

To allow the model development process to extract maximum information with minimum number of experiments, a statistically designed experiment was performed. A 2^{5-1} fractional factorial experiment was chosen for experimental design. The numerical values of the range of five design variables are summarized in Table 1. The length of the structure was chosen such that the variation of *s*-parameters did not contain any singularities up to 35 GHz. The mounted CPW lines had a length of 100 mils, and the bottom substrate lines were 50-mil long with 50-Ω characteristic impedance.

Table 1. Range of Layout Parameters for the Experiment

Input Variable	**Low Level (μm)**	**High Level (μm)**
Bump height (*h*)	20	100
Bump diameter (*a*)	30	100
CPW width (*w*)	150	250
Bump-to-edge distance *d*)	25	100
Conductor Overlap (*o*)	150	300

To characterize and analyze the electrical behavior of flip chip transitions, the lumped equivalent circuit is the simplest and most accurate method [48]. System performance can be characterized by *s*-parameters. The output variables for the experiment were S_{11} (dB) (reflection coefficient) and S_{21} (dB) (insertion loss). Since the structure is symmetrical, $S_{11} = S_{22}$ and $S_{12} = S_{21}$. The *s*-parameters obtained were then used to derive the inductance (L) and capacitance (C1 = C2 = C) values of the π lumped element model shown in Figure 7. Thus, all the required components for the complete characterization of the electrical behavior of the flip chip transitions were extracted.

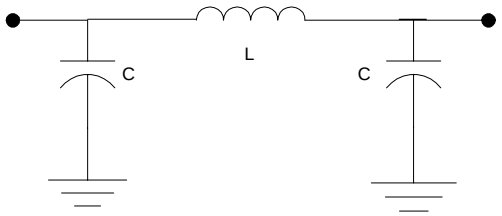


Figure 7. Lumped element model of flip chip transition.

3.2. Fabrication and Data Acquisition

RF test structures were fabricated and measured to validate FEM simulations. The test board is shown in Figure 8. Test samples utilized substrates and die made from 99.6 % alumina, which were 10 mils thick with 0.05 mils of sputtered Au. The substrates were bumped with 1 mil wire (99% Au 1% Pd). Bump sizes ranged from 66-70μm in diameter and 43-47μm in height. The dice were attached to the bumped substrates by a thermo sonic flip-chip process using an SEC Model 410 Flip-Chip Bonder. This process uses a combination of heat, pressure and ultrasonic energy to form a bong between the bump and the metallization on the joining surface. The process conditions used were 180°C base temperature, 50g per bump force, and a system power setting of 6 on a 40-watt ultrasonic power generator. Based on samples created during the building of these test structures, the bump interconnect had a standoff height of 20 - 30μm and a sheer strength of approximately 30gms per bump.

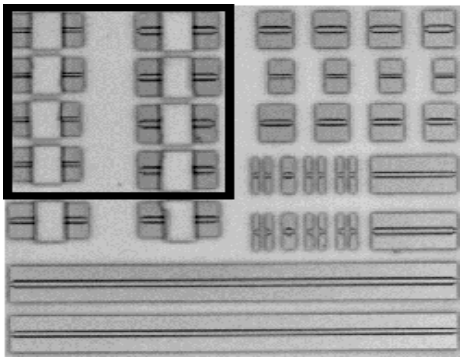
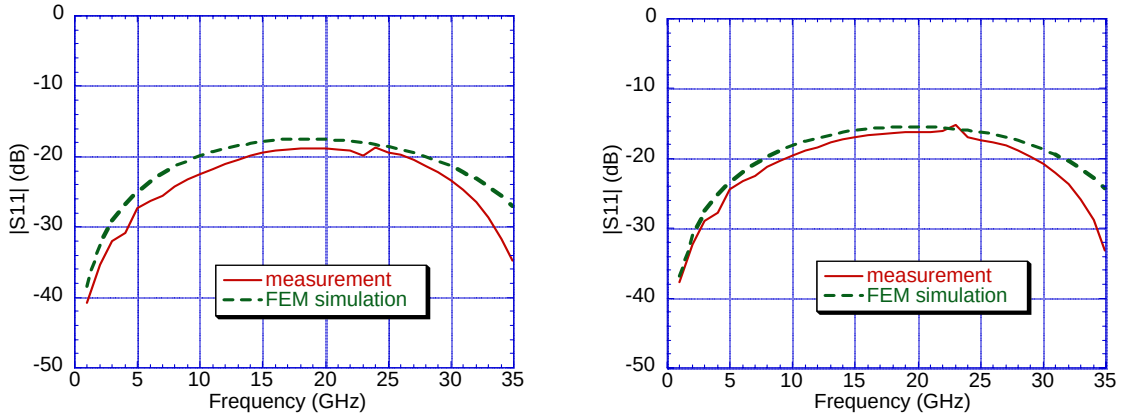


Figure 8. Microphotograph of the test board.

Full-wave finite-element simulations were performed using Agilent's *High Frequency Structure Simulator* [49]. The simulated data is shown in Table 2. Data obtained from the FEM simulations were verified by measurements of test structures. These measurements were performed using an HP8510B network analyzer with on-wafer ground-signal-ground probes. All structures were measured with 150μm probe pitches. The wide CPW lines were tapered. A line-reflect-match (LRM) calibration was used for the narrow lines, and custom thru-reflect-line (TRL) calibration was used for de-embedding the effect of tapering for the wide CPW lines [50].

The measured and simulated output electrical variables were S_{11} and S_{21}. Figure 9 shows the measured and simulated values of S_{11} for two different layouts. The measured values and the FEM simulations match closely in the frequency range of 1-35 GHz. The fabrication process did not provide variation of bump height and bump diameter, so FEM simulations were used for model development, as they matched the values obtained for similar fabricated samples. For model development purposes, the *s*-parameter values were selected at 20 GHz.



a). (d = 200μm, o = 120μm) *b). (d = 200μm, o = 120μm).*

Figure 9. Measured and simulated values of S_{11}

Table 2. Fractional Factorial Experimental Data For Flip Chip Transitions

Run	**Inputs (μ m)**					**Outputs**			
	h	*a*	*w*	*d*	*o*	*L* (pH)	*C* (fF)	$\|S_{11}\|$ (dB) @ 20GHz	S_{22}| (dB) @ 20 GHz
1	20	30	150	25	300	90	43	-16.642	-0.095
2	100	30	150	25	150	90	33	-21.009	-0.035
3	20	100	150	25	150	50	24	-21.288	-0.032
4	100	100	150	25	300	100	53	-14.430	-0.159
5	20	30	250	25	150	72	25	-23.844	-0.018
6	100	30	250	25	300	130	48	-18.241	-0.066
7	20	100	250	25	300	90	42	-16.986	-0.088
8	100	100	250	25	150	75	28	-22.100	-0.027
9	20	30	150	100	150	63	25	-21.414	-0.025
10	100	30	150	100	300	110	47	-16.862	-0.090
11	20	100	150	100	300	82	42	-16.369	-0.101
12	100	100	150	100	150	72	30	-20.502	-0.039
13	20	30	250	100	300	80	38	-17.631	-0.076
14	100	30	250	100	150	87	24	-28.189	-0.007
15	20	100	250	100	150	38	20	-22.278	-0.026
16	100	100	250	100	300	95	45	-16.361	-0.102

3.3. Neural Network Modeling

The goal of neural network modeling was to develop an accurate mapping of the relationship between the flip chip layout parameters and electrical performance. Different neural networks were used for modeling each of the four electrical parameters: S_{11}, S_{21}, L, and C. Each of the four neural networks used had three layers. Each input layer had five neurons, corresponding to the five geometrical parameters varied in the experiment. The number of neurons in the hidden layer was varied and selected based on the accuracy of the model. The output layer consisted of a single neuron representing the appropriate electrical response. Network training was accomplished using the Object-Oriented Neural Network Simulator (*Obornns*) a Java-based software package developed by the Intelligent Semiconductor Manufacturing group at Georgia Tech [51]. Seventy-five percent of the data was used to train the models, and the remaining 25% of the data was used for validation. Several configurations of neural networks and different values of learning rate were investigated to obtain optimal results. The momentum term was discarded in this model development process. The modeling results are summarized in Table 3. In this table, network structure is depicted as *x-y-z,* where *x* denotes number of neurons in the input layer, *y* is the number of neurons in the hidden layer, and *z* is the number of neurons in the output layer.

The modeling results indicate prediction errors from 3 - 17%. This accuracy is reasonable, considering the fact that the test data set was at the boundary of the training data. The trained neural networks were used to further study the impact of various layout parameters on the electrical properties of the flip chip transitions.

Table 3. Optimized Flip Chip Neural Network Parameters

Output variable	**NN structure *x-y-z***	**Learning rate (η)**	**RMSE Prediction Error**	**Prediction Error (%)**
L	5-5-1	0.01	5.7	4.71%
C	5-3-1	0.01	2.03	3.65%
$\|S_{11}\|$	5-5-1	0.01	0.817	2.22%
$\|S_{21}\|$	5-7-1	0.01	0.020	16.6%

3.4. Statistical and Sensitivity Analysis

An analysis was initially performed to establish the statistical significance of the layout parameters. The *F*-statistics are shown in Table 4. The threshold value of *F* for statistical significance at a 95% confidence level was calculated to be 3.2. The conductor overlap is the most significant layout parameter for all the electrical components. It is noteworthy that a higher statistical significance of a layout parameter for an electrical characteristic implies that layout parameter is the most sensitive. For instance the F-statistic is high for the conductor overlap, and so is the sensitivity. Similarly, the bump height is statistically insignificant for $|S_{11}|$, and the bump height is insensitive to $|S_{11}|$. Similar results can be obtained for other parameters.

Table 4. F-*statistic for the Layout Parameters*

Layout Parameter	L	C	$\|S_{11}\|$	$\|S_{12}\|$
Bump height (*h*)	65.7	14.0	0.1	1.4
Bump diameter (*a*)	19.5	0.0	8.9	9.3
CPW width (*w*)	0.1	4.0	14.9	9.8
Bump-to-edge distance *d*)	6.1	3.4	1.2	1.0
Conductor Overlap (*o*)	114.1	740.4	373.9	460.2

Sensitivity analysis for the flip chip transition models was performed by examining the mean of the layout parameter and making incremental changes in the input of interest. The values of the outputs were normalized. In this case, sensitivity has been calculated by varying the input parameters by 10% of their full range of deviation. The results of the normalized sensitivity analysis are shown in Figures 10-13.

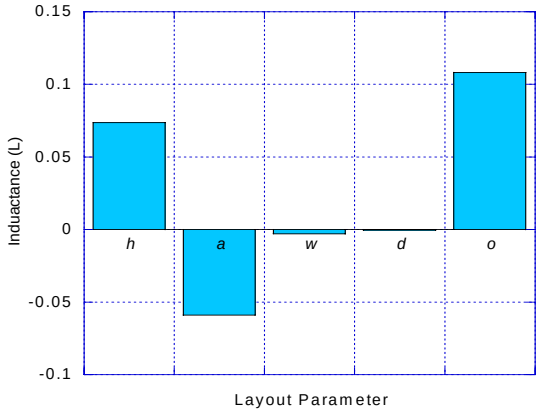


Figure 10. Sensitivity of inductance.

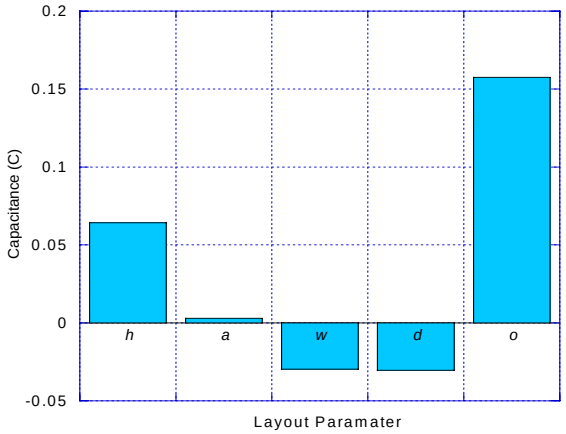


Figure 11. Sensitivity of capacitance.

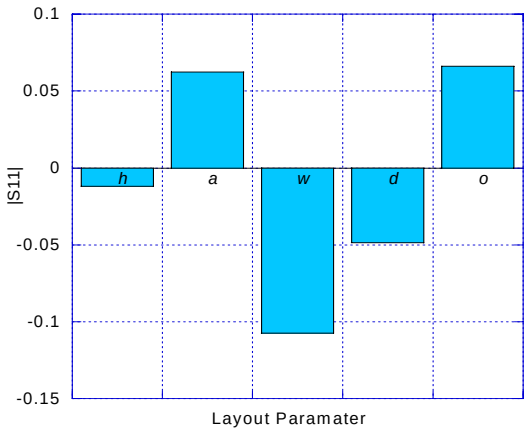


Figure 12. Sensitivity of $|S_{11}|$.

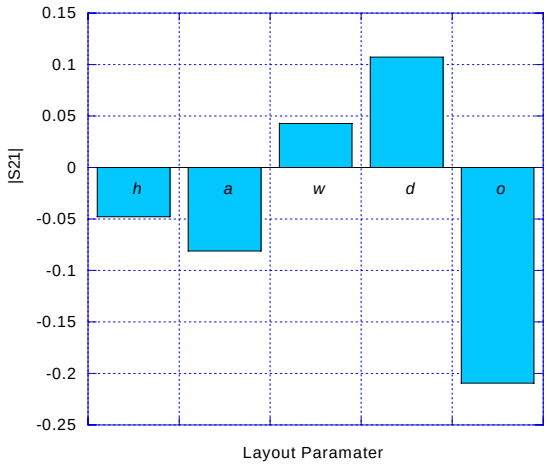


Figure 13. Sensitivity of |S21|.

The results of sensitivity analysis reveal the impact of design parameters on electrical performances. The inductance of the flip chip transition is most sensitive to bump height, diameter and overlap of the top and bottom CPW lines. Furthermore, inductance increases with bump height and conductor overlap and decreases with an increase in bump diameter. This is expected because with increase in bump height, the electrical signal path of the transitions increases, thereby causing an increase in inductance. This underscores the importance of short bumps to reduce electrical inductance. Inductance decreases with the bump diameter because the cross sectional area of the signal line

increases, hence reducing the electrical inertia (inductance). Finally, inductance decreases as *d* increases because the effective distance between ground and signal bump increases, hence reducing mutual inductance. The simplified equation for the self-inductance for a cylindrical bump is given as [52]

$$L = \frac{\mu_0 h}{2\pi}\left[\ln\left\{\frac{2h}{d}+\sqrt{\left(1+\frac{4h^2}{d^2}\right)}\right\}-\sqrt{\left(1+\frac{d^2}{4h^2}\right)}+\frac{d}{2h}\right] \tag{11}$$

where *h* is the bump height and *a* is the bump diameter. This equation is valid for a single isolated bump, but illustrates that bump height and diameter have significant impact on inductance. The capacitance is most sensitive to conductor overlap. It increases with overlap because more overlap results in greater capacitance between top and bottom lines. The capacitance decreases with an increase CPW line width and line edge to ground bump distance. Capacitance increases with bump height, as the electrical signal path increases, and hence, the shunt capacitance increases.

The magnitude of the *s*-parameters is also sensitive to the layout parameters to varying degrees. The relationship between *s*-parameters and the lumped element model of Figure 7 can be obtained using Kirchoff's Laws as

$$S_{11} = \frac{j\omega LC\left[\frac{1}{C}-\frac{2Z_0^2}{L}+\omega^2 CZ_0^2\right]}{2Z_0(1-\omega^2 LC)+j\omega LC\left[\frac{1}{C}+\frac{2Z_0^2}{L}-\omega^2 CZ_0^2\right]} \tag{12}$$

$$S_{12} = \frac{2Z_0}{2Z_0(1-\omega^2 LC)+j\omega LC\left[\frac{1}{C}+\frac{2Z_0^2}{L}-\omega^2 CZ_0^2\right]} \tag{13}$$

where Z_0 is the reference impedance (usually 50 Ω) and L and C are the lumped element components values from Figure 7. The most important result is the lack of sensitivity of

$|S_{11}|$ to bump height, since the repeatability of bump height is major concern below 100 μm. The s-parameters are most sensitive to variations in conductor overlap. Another interesting observation is that while CPW transmission line launch parameters, namely *w* and *d*, do not have very significant impact on lumped electrical model components, but have significant impact on s-parameters. This can probably be attributed to the fact that the transmission line launch affects the matching characteristics of the circuit. On the contrary, the bump dimensions, namely *h* and *a*, have greater impact on lumped element electrical components rather than on s-parameters.

The results of sensitivity analysis show that geometrical dimensions impact the electrical characteristics of the of the signal path. Variations in these dimensions can lead to variations in electrical performance. For example, such variations can lead to frequency shifts in voltage-controlled oscillators due to interconnect parasitics, particularly in the GHz range. They can also alter the matching impedance of power amplifiers and degrade their performance. In order to overcome this problem, suitable optimization must be performed to extract the appropriate electrical design parameters so that circuits will be immune to interconnect parasitics and performance degradation can be minimized.

3.5. Response Surface Plots

To observe the variation of the *s*-parameters and lumped circuit components along the entire range of layout parameters, 3-D response surface plots were obtained from the neural network models (see Figures 14-17). The other layout parameters were kept at their mean values.

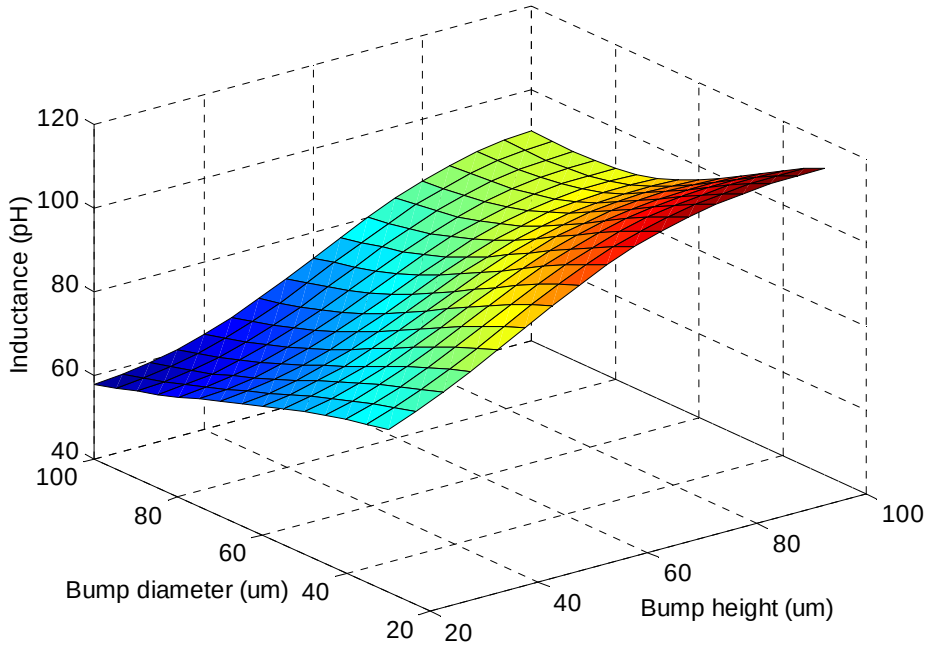


Figure 14. 3-D contour plot of inductance.

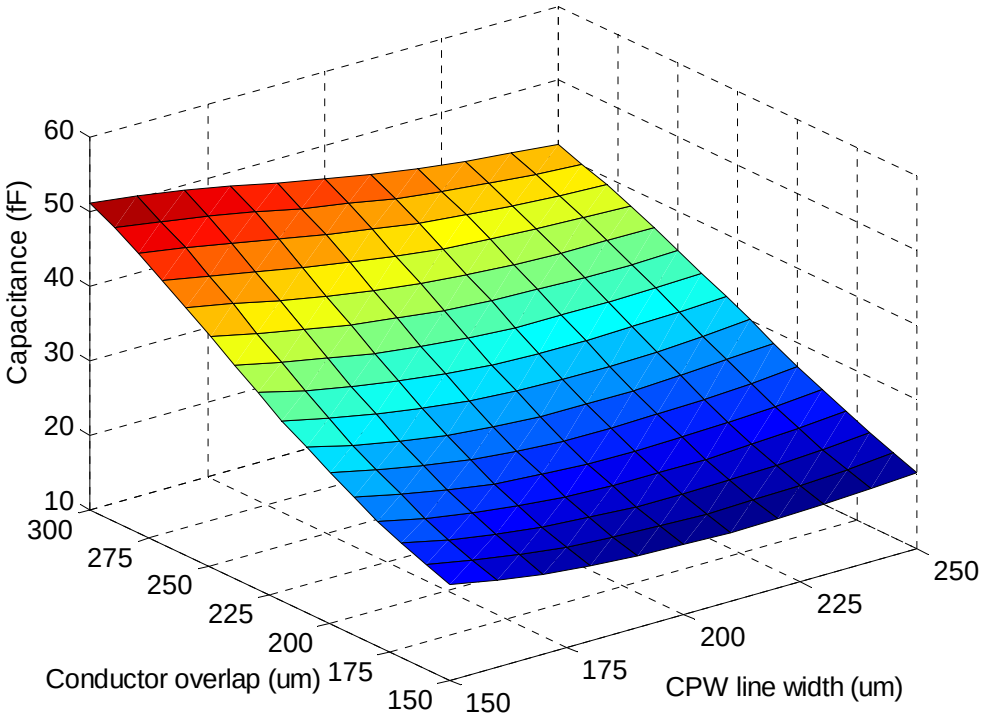


Figure 15. 3-D contour plot of capacitance.

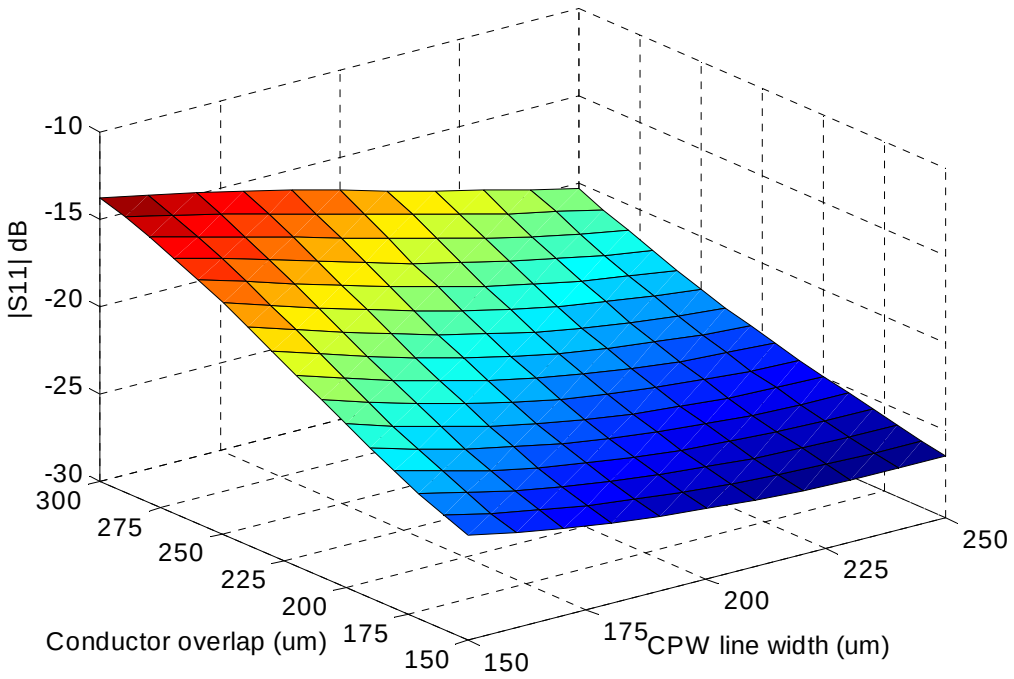


Figure 16. 3-D contour plot of $|S_{11}|$.

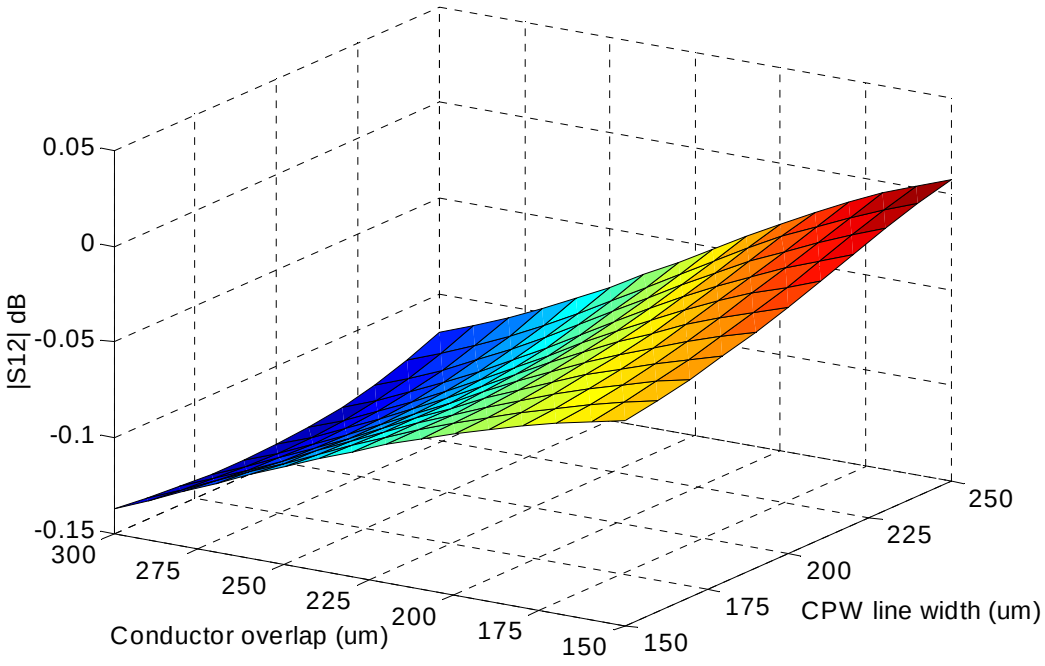


Figure 17. 3-D contour plot of $|S_{21}|$.

Figure 14 shows that inductance increases with bump height because of greater conductor length. The inductance decreases due to increase in bump diameter because of reduced inertia. However, the change in inductance with bump diameter is not as pronounced as compared to bump height. Thus, in order to reduce inductance, bump height should be minimized. Figure 15 reveals that capacitance increases with conductor overlap and is reduced slightly with an increase in CPW line width.

The response surface plot for $|S_{11}|$ in Figure 16 shows an increase with conductor overlap. The $|S_{11}|$ value also increases with CPW line width for lower values of conductor overlap, but decreases at higher values. This is due to different matching conditions at different values of conductor overlap. This illustrates that to achieve desired low values of $|S_{11}|$, the conductor overlap should be minimized and an optimal value of CPW line width should be identified. Figure 17 shows that greater conductor overlap results in a decrease in $|S_{21}|$. CPW line width, on the other hand, can increase or decrease $|S_{21}|$, depending on the matching conditions. In order to avoid insertion loss and obtain an $|S_{21}|$ value close to 0 dB, the conductor overlap should be minimized and appropriate vales of CPW line width should be identified.

3.6. Summary

Neural network modeling of flip chip transitions is presented in this chapter. The models obtained are accurate to within 5 - 15% for mapping bump geometry to various electrical characteristics. The models were used to perform sensitivity analysis and generate 3-D contour plots of the electrical characteristics. The lumped element electrical model of the flip chip interconnect transition has been characterized from 1 - 35 GHz.

The return (S_{11}) and insertion losses (S_{21}) have been fully characterized at a frequency of 20 GHz. However, this model can be extended to model the *s*-parameters from 1 - 35 GHz.

Analysis of the results shows that the conductor overlap is the most significant design parameter for the flip chip interconnection. The model obtained can be used for optimization of electrical parameters. The model can also be used to obtain the necessary layout parameters for a set of desired electrical characteristics using the response surface plots.

CHAPTER 4

Design of Multilayer RF Passives

Multilayer integrated RF passives have been proposed as a superior technology over conventional surface mount technology. They have become a primary focus on research due to the real estate efficiency, cost-savings, size reduction, and performance improvement resulting from inherent capability for easy integration [53]. However, the three dimensional (3-D) integration approach produces passives with complex topology and is difficult to model and optimize. The method of moments (MOM) [54] is suitable for modeling planar structures like transmission lines, but not suitable for these types of devices. Full wave 3-D electromagnetic field solvers are required, but these consume enormous amount of time. In this chapter, the neuro-genetic optimization method is applied to modeling, analysis, and design of multilayer inductors and capacitors for W-CDMA (1.9 GHz) and C Band (2.4 GHz) applications. The examples in this chapter illustrate the use of the neuro-genetic algorithm in the post-fabrication stage to reduce the cost and effort in the iterative loop 2 shown in Figure 5.

4.1. Experimental Design

Inductors with values of 4-12 nH and capacitors with values of 1-10 pF typically cannot be fabricated on-chip and require off-chip or system-on-package (SOP) implementation. The operational frequency range considered for the inductors and capacitors in this study was 1-5 GHz, which is suitable for W-CDMA (1.9 GHz) and

802.11b wireless LAN (2.4 GHz) applications. The inductors were single-turn square devices with all four sides on different metal layers of the substrate, as shown in Figure 18. This compact inductor topology occupies 75% less area compared to a planar layout [55]. The capacitors were square, parallel-plate devices. Such a topology is difficult to model and optimize using conventional modeling techniques because of its 3-D structure and vertical vias. It is also therefore a good candidate for neural network modeling.

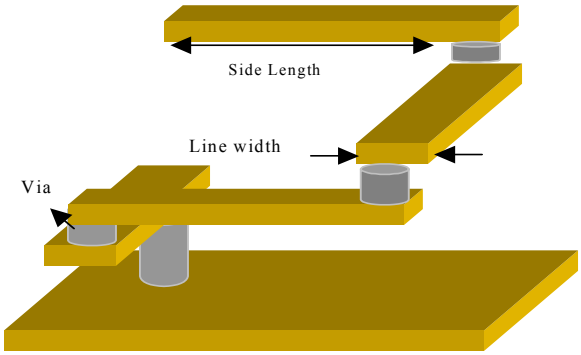


Figure 18. Inductor schematic.

Initial EM simulations were performed to determine the approximate range of layout parameters (Table 5) that yield inductance values of 4-12 nH (with a high quality factor) and capacitance values of 1-10 pF at 1.9 GHz (W-CDMA) and 2.4 GHz (802.11b WLAN). Latin hypercube sampling was used for experimental design.

Table 5. Range of Passive Layout Parameters

Type	Side Length	Line Width
Inductor	1000-5000 μm	350-500 μm
Capacitor	1000-5000 μm	-

4.2. Fabrication and Measurements

The parallel plate capacitors and spiral inductors were fabricated using a 12-metal layer low temperature co-fired ceramic (LTCC) process. The LTCC substrate used in the

fabrication had a dielectric constant of 5.2 and a loss tangent of 0.0012. The samples were fabricated at Asahi Glass Company. The fabricated samples are shown in Figure 19. One-port electrical measurements were performed using LRRM calibration with a calibration error of +/- 0.01 dB [56]. The quality factor and the component values were obtained from *s*-parameters using Equations (14)-(16). Electrical parameters were extracted at 1.9 GHz and 2.4 GHz. The measurement results for some sample devices are shown in Figures 20-22. The value of the Q factor becomes negative at the self-resonant frequency of inductor. The self-resonant frequency is above 3 GHz for all devices, thus making them suitable for operation at 1.9 GHz and 2.4 GHz. The quality factors obtained were up to 100. The inductance and capacitance values for various devices were in the range of 4-12 nH and 1-10 pF, respectively. The extracted values for inductance and capacitance are shown in Table 6 and 7 respectively.

$$L_{eff} = \frac{imag\left(Z\left(11\right)\right)}{2\pi f} \tag{14}$$

$$C = \frac{imag\left(Y\left(11\right)\right)}{2\pi f} \tag{15}$$

$$Q(inductor) = \frac{imag\left(Z\left(11\right)\right)}{real\left(Z\left(11\right)\right)} \tag{16}$$

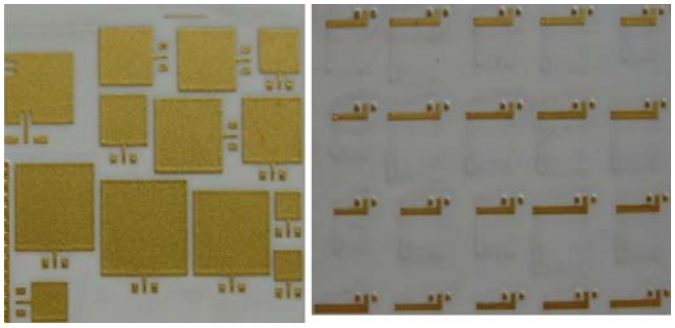


Figure 19. Fabricated samples of capacitors and inductors.

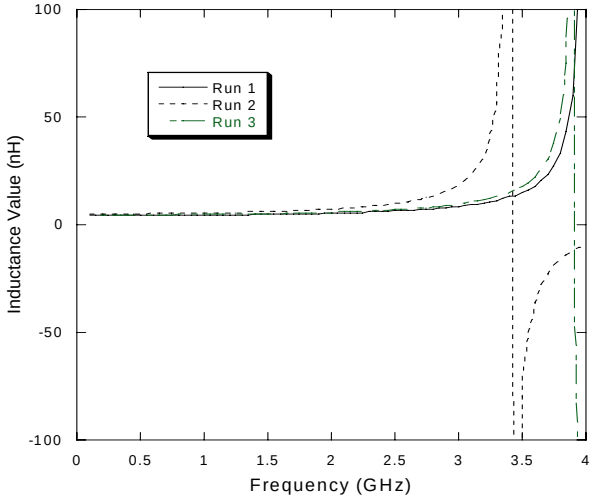


Figure 20. Inductance vs. frequency for the sample inductors.

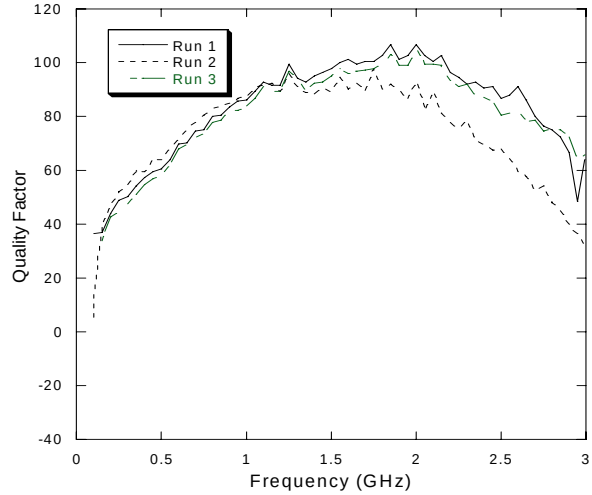


Figure 21. Quality factor vs. frequency for the sample inductors.

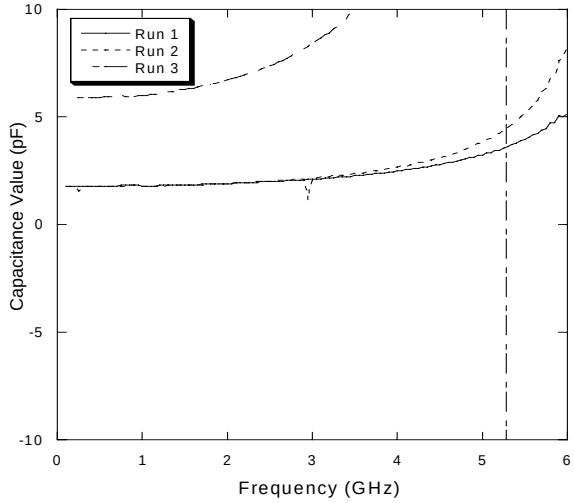


Figure 22. Capacitance vs. frequency for the sample capacitors.

Table 6. Experimental Data for Inductors

Run	Layout Parameter (μ m)		Electrical Parameters				
#	Line Width	Side Length	L_{eff} @ 1.9 GHz (pH)	Q-factor @ 1.9 GHz	L_{eff} @ 2.4 GHz (pH)	Q-factor @ 2.4 GHz	SRF (GHz)
1	500	1500	4.228	77.388	4.724	80.243	4.51
2	500	2350	7.677	87.979	10.82	63.297	3.2
3	450	2150	6.662	91.969	8.532	75.654	3.5
4	450	2650	9.586	81.891	15.91	46.942	2.92
5	450	2200	6.98	89.726	9.098	69.792	3.42
6	450	2500	8.643	85.044	12.97	53.363	3.05
7	450	2900	11.68	74.056	25.23	29.458	2.71
8	450	2250	7.251	95.686	9.742	70.258	3.34
9	450	1800	5.268	101.22	6.174	90.699	4
10	400	2500	8.711	91.25	12.6	63.463	3.15
11	400	1850	5.482	100.76	6.483	73.328	3.97
12	400	1900	5.675	99.292	6.706	87.264	3.94
13	400	2700	10.08	83.884	16.53	52.059	2.94
14	400	2850	11.35	81.962	21.54	40.53	2.79
15	400	2000	6.102	102.081	7.424	101.41	3.75
16	400	2450	8.334	95.404	11.78	75.301	3.18
17	400	2100	6.864	81.931	8.686	70.446	3.55
18	350	1750	5.784	67.126	6.644	45.864	4.18
19	350	1650	-	-	-	-	-
20	500	2750	11.22	69.18	22.25	36.075	2.76

Table 7. Experimental Data for Capacitor

Run	Layout Parameter (μ m)	Electrical Parameters	
#	Side Length	Capacitance @ 1.9 GHz	Capacitance @ 2.4GHz
1	2500	4.437	4.873
2	2700	5.342	6.067
3	1900	2.516	2.686
4	2200	3.468	3.849
5	3150	7.754	9.395
6	2800	6.102	7.319
7	4000	-	-
8	3550	12.533	19.39
9	1250	1.068	1.091
10	1350	1.238	1.274
11	3650	12.89	-
12	1700	1.894	1.977

4.3. Neural Network Modeling

Measured parameter values are used to develop neural networks models of inductor and capacitor performance. The neural network model was thus able to capture fabrication variations. No assumption regarding the substrate behavior or metal traces was made. Seventy-five percent of the data was used for training, and 25% was used for testing. Individual neural networks were derived for each performance parameter to attain greater accuracy. The results are shown in Table 8. The *x-y-z* values of neural structure in this table refer to the number of neurons in the input, hidden, and output layers, respectively. The neural network structure and learning parameters were optimized to obtain high accuracy with minimal training. The neural network had an average

prediction error of less than 5%. The quantity factor prediction error is slightly higher due to error involved in measurement of high value of inductance of the order of 100.

Table 8. Neural Network Parameters for Inductor and Capacitor Modeling

Output Parameter	**NN Structure**	**Learning rate (η)**	**Prediction Error**	
			RMSE	**% RMSE**
Inductor L (1.9 GHz)	2-7-1	0.01	0.008	0.952
Inductor Q (1.9 GHz)	2-9-1	0.05	8.04	6.33
Inductor L (2.4 GHz)	2-7-1	0.01	0.056	4.21
Inductor Q (2.4 GHz)	2-9-1	0.05	10.93	8.08
Inductor SRF	2-7-1	0.01	0.059	0.295
Capacitor C (1.9GHz)	1-9-1	0.05	0.638	3.7
Capacitor C (2.4 GHz)	1-9-1	0.05	1.943	7.5

4.4. Sensitivity Analysis and Response Surface Plots

Sensitivity analysis for the inductor performance parameters was performed by using the mean value of the layout parameters and making incremental changes (10% of their full range of deviation) in the input of interest. Normalized results of the sensitivity analysis are shown in Figure 23. Similar analysis was not performed for the capacitors because they have only a single layout parameter to vary. This analysis reveals that inductance is most sensitive to the side length of the square spiral. This was expected, since with an increase in side length, the effective radius and flux increased (and hence, inductance). The SRF is sensitive to side length, as the increasing the size of the inductor makes it more capacitive. The quality factor is most sensitive to line width, decreasing with increasing line width since increasing its area makes the device more capacitive.

However, with an increase in length, Q increases slightly, since the imaginary part of Z_{11} increases with inductance.

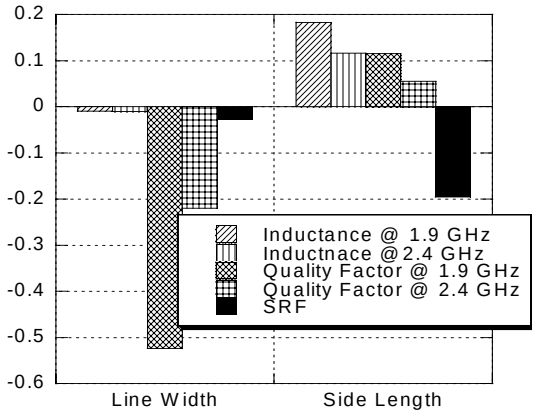


Figure 23. Sensitivity analysis for the inductor.

To graphically illustrate trends in the variation of inductance, Q-factor, and SRF along the range of layout parameters studied, 3-D response surface plots were generated from the neural network models (Figures 24-26). Figure 24 indicates that SRF decreases with an increase in the side length and remains fairly independent of line width. However, Figure 25 shows that inductance increases with side length and decreases slightly with line width. The latter effect is likely due to an increase in the capacitive coupling between the ground plane and the device [57]. Figure 26 reveals that the Q-factor has a very nonlinear relationship with variations in layout. Because of the complex dynamics of resistive losses associated with metal strips, such a result is not unexpected [58]. Also, since the Q-factor is on the order of 100, the values are noisy due to measurement errors. Losses are frequency and geometry-dependent and are directly related to the Q-factor of the inductor coil. The Q-factor generally decreases with increases in line length due to increases in resistance. High values of Q are obtained at intermediate values of side length and line width.

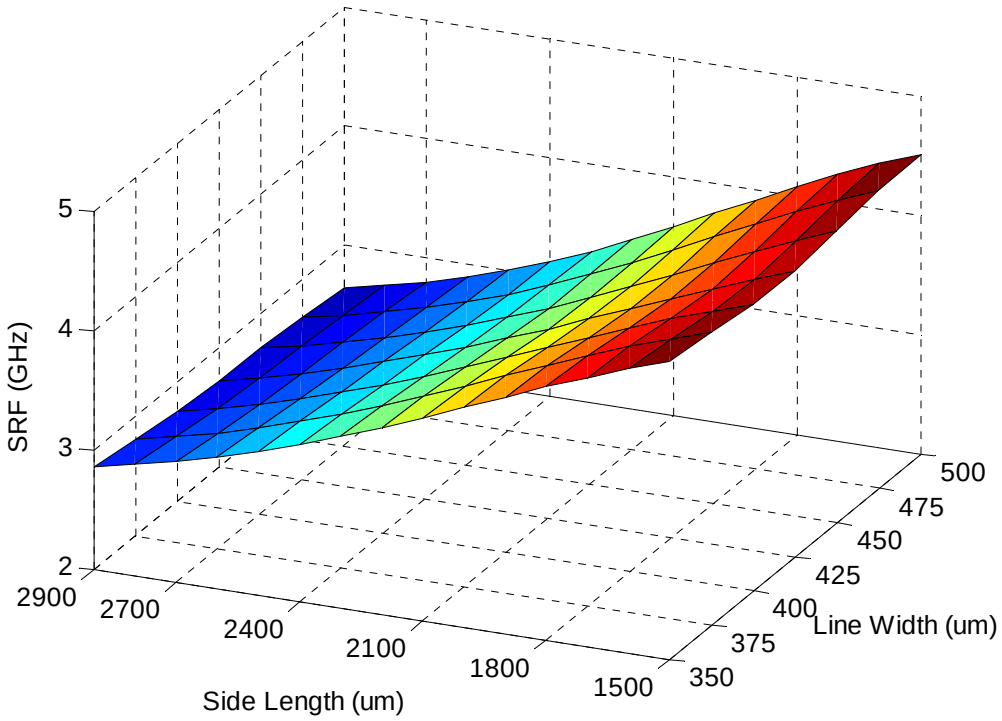


Figure 24. SRF vs. for the inductor.

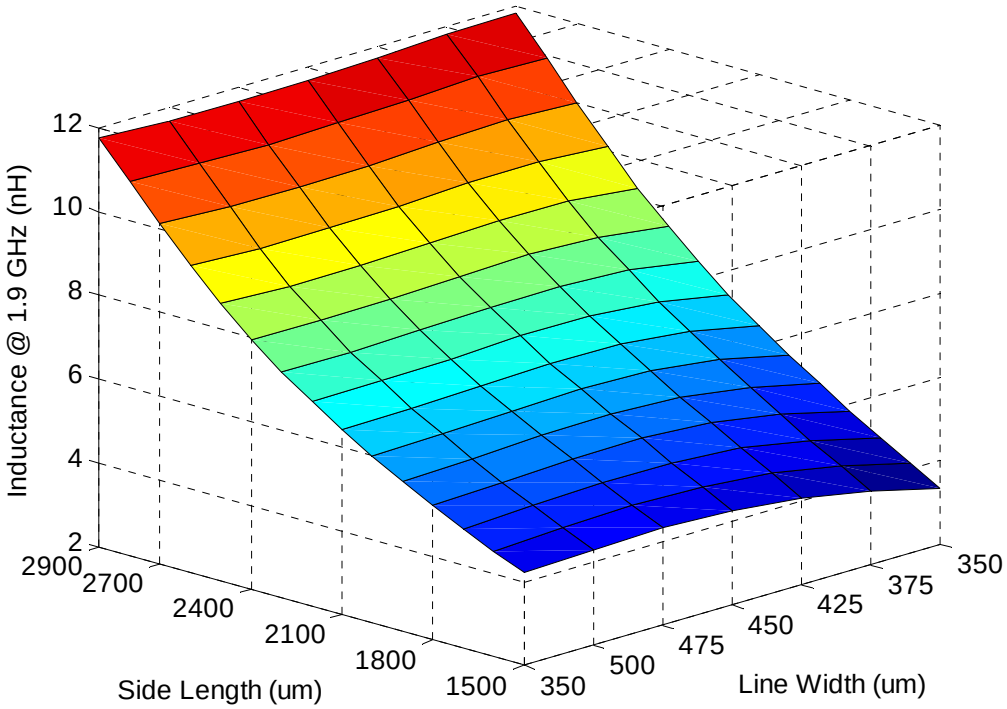


Figure 25. Inductance vs. for the inductor.

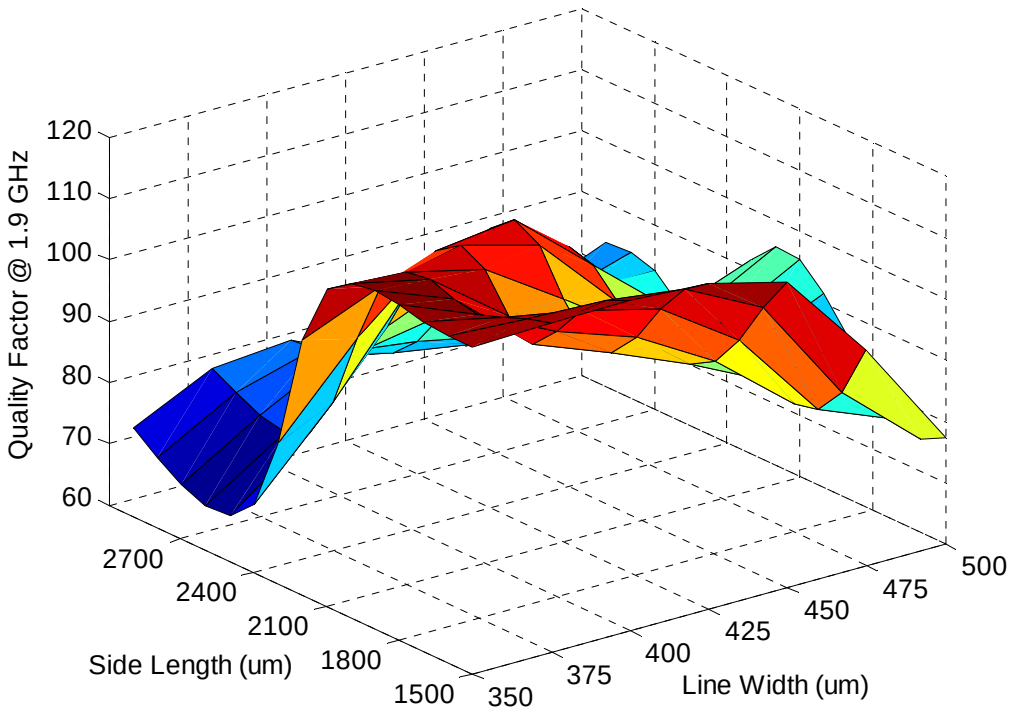


Figure 26. Quality factor vs. for the inductor.

4.5. Neuro-Genetic Optimization

Neuro-genetic optimization was performed to determine the layout parameters that give the desired electrical performance. The desired electrical parameters for a device were provided to the genetic optimizer. The genetic optimizer, using the neural network model of the search space, determined the set of layout parameters that gave (or were close to) the desired electrical responses. The genetic algorithm parameters (shown in Table 9) were chosen to obtain sufficient accuracy with minimum number of iterations. All electrical performance parameters for inductors and capacitors were assigned equal weights during optimization.

Table 9. Genetic Algorithm Parameters for Inductor and Capacitor Design

Genetic Algorithm Parameter	Value
Crossover Probability	0.65
Mutation Probability	0.01
Population Size	100
Chromosome Length	100

The results of neuro-genetic design optimization for the capacitors and inductors are shown in Tables 10 and 11, respectively. Since the board was fabricated prior to optimization, test structures were fabricated to verify the design. The measured electrical parameter values of the test structures were provided to the neuro-genetic optimizer to predict the optimum layout. The layout values for those electrical responses were very close to the actual layout values used. For a targeted capacitance of 4.4 pF at 1.9 GHz the neuro-genetic optimizer predicts a side length of 2502 μm, which is close to actual value of 2500 μm. Similarly for a capacitance of 3.8 pF, the algorithm predicts a layout of 2206 μm, which is close to the actual value of 2200 μm. If one considers the fabrication tolerances for LTCC samples, the difference of 2 and 6 μm are negligible. For inductor design, there are three electrical parameters. For a target inductance of 10.1 nH with a Q-factor of 84 and SRF of 2.94, the optimizer predicts layout parameters of 418 μm (line width) and 2687 μm (side length), which are close to the actual values of 400 μm and 2700 μm, respectively. Similar results were obtained for other targeted electrical specifications. Thus, this approach was effective in predicting the layout values for a desired electrical response.

Table 10. Neuro-Genetic Optimization of Capacitors

		Capacitance (pF)	Side Length (μm)
1	Actual/Target	4.4 @ 1.9 GHz	2500
	NN-GA	4.5 @ 1.9 GHz	2502
2	Actual/Target	3.8 @ 2.4 GHz	2200
	NN-GA	3.4 @ 2.4 GHz	2206

Table 11. Neuro-Genetic Optimization of Inductors

Optimization (@ 1.9 GHz)		**L (nH)**	**Q**	**SRF (GHz)**	**Line Width, Side Length (μm)**
1	Actual	10.1	84	2.94	400,2700
	NN-GA	10.0	84	2.93	418,2687
2	Actual	5.3	101	4	450,1800
	NN-GA	5.5	100	3.96	425,1832
Optimization (@ 2.4 GHz)		**L (nH)**	**Q**	**SRF (GHz)**	**Line Width, Side Length (μm)**
1	Actual	16.5	52	2.94	400,2700
	NN-GA	16.9	49	2.96	462,2653
2	Actual	6.2	91	4	450,1800
	NN-GA	6.2	92	3.97	422,1842

An innovative neuro-genetic optimization technique has been used for modeling, and optimization of multilayer inductors and capacitors. The algorithm was used in post-fabrication stage in the microwave design flow. This enabled the model to capture the manufacturing variations and other effects that could not be modeled by electro-magnetic simulator. The neuro-genetic optimization results were accurate and efficient in predicting the layout for desired electrical characteristics. The inductor performance parameters - quality factor, self-resonant frequency and effective inductance - could be modeled, and layout parameters (for desired electrical response) could be predicted with

greater than 95% accuracy. Similar accuracy was obtained for capacitors. Overall, this methodology is a powerful tool for optimizing the design of RF passives post fabrication and fine tunes the design variables prior to high volume manufacturing. The generic nature of the technique suggests potential extension to other complex topologies, including band pass filters, diplexers, and active microwave circuits.

CHAPTER 5

Filter Synthesis

Microwave filters are an important component in wireless communication systems. Compact, integrated, and low-cost filter design for optimal electrical performance has been a challenge to microwave designers. Filter design involves several trade-offs between various design parameters. There are always two or more performance parameters for which improvement in one leads to deterioration of other parameters. For example, narrow bandwidth leads to greater pass band insertion loss and vice-versa. Furthermore, compact bandpass filters such as those discussed in this chapter have complex folded structures, which are difficult to model and synthesize. Mm-wave filters are even more challenging to design. At mm-wave frequencies there is an appreciable performance shift (from targeted response) after fabrication due to process variations and other effects that can not be modeled and accounted for in EM tool-based pre- fabrication design. Therefore, there is a need to determine a precise set of layout parameters that meets desired electrical specifications (such as operating frequency, bandwidth, insertion loss, etc.). The algorithm for synthesizing such a design should be highly accurate, but not overly time-consuming.

In this chapter, neuro-genetic design is used in the post fabrication stage to synthesize low pass filters in the range of 40-60 GHz. A compact bandpass filter design for a frequency range of 5-6 GHz for 802.11a/ HIPERLAN2 wireless LAN applications is also presented. In bandpass filter design, the neuro-genetic methodology is used in the iterative loop 1 (Figure 5) involving CAD tools. Computational cost comparisons are

performed between the proposed method and popular CAD tools using the bandpass filter examples.

5.1. MM-wave Filter Synthesis

The neuro-genetic methodology is applied for mm-wave filter synthesis in the range of 40-60 GHz. This frequency band is suitable for remote sensing and emerging 60 GHz wireless LAN applications. In this section, the proposed method is used to fine tune mm-wave low pass filter response to desired electrical target from the measurement data.

5.1.1. Experimental Design and Data Acquisition

A prototype low pass filter was designed by combining in cascade the constant-k, m-derived sharp cutoff, and the m-derived matching sections [59]. Such a composite topology can be used to realize a filter with the desired attenuation and matching properties. The filters were designed to obtain a cut off frequency in the range of 35-70 GHz and an input impedance of 50 Ω. This filter was realized using the microstrip transmission line configuration. The various layout parameters of the filter are shown in Figure 27. Some of these parameters were kept constant to reduce complexity in modeling and optimization. Latin hypercube sampling was again used for experimental design.

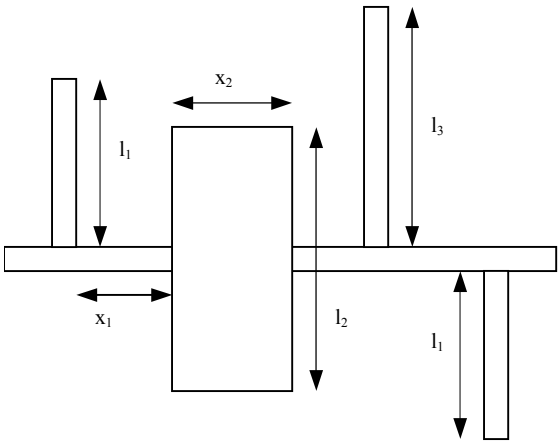


Figure 27. Layout schematic of mm-wave low pass filter.

Initial EM simulations were performed to obtain the approximate range (Table 12) of five layout parameters that would give a cutoff frequency between 35-70 GHz, low insertion loss in the pass band, and good rejection in the cutoff range. The range of the layout parameters is shown in Table 12.

Table 12. Range Of Layout Parameters for Low-Pass Filter

Layout Parameter	**Low (μm)**	**High (μm)**
l_1	350	550
l_2	400	600
l_3	450	800
x_1	300	500
x_2	200	400

The mm-wave low-pass filter was fabricated using a 12-metal layer LTCC process. Microstrip lines were fabricated on the top metal layer, with the second metal layer as a ground plane connected with vertical vias. Fabricated filter samples are shown in Figure 28. Two-port electrical measurements were performed using LRRM calibration on a network analyzer. The measured values for a sample filter are shown in Figure 29. The measurement exhibits the required low insertion loss in the pass band and a high rejection in the cutoff range. The extracted measured data is shown in Table 13.

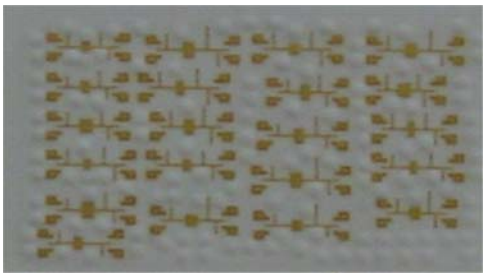


Figure 28. Fabricated samples of mm-wave low pass filters.

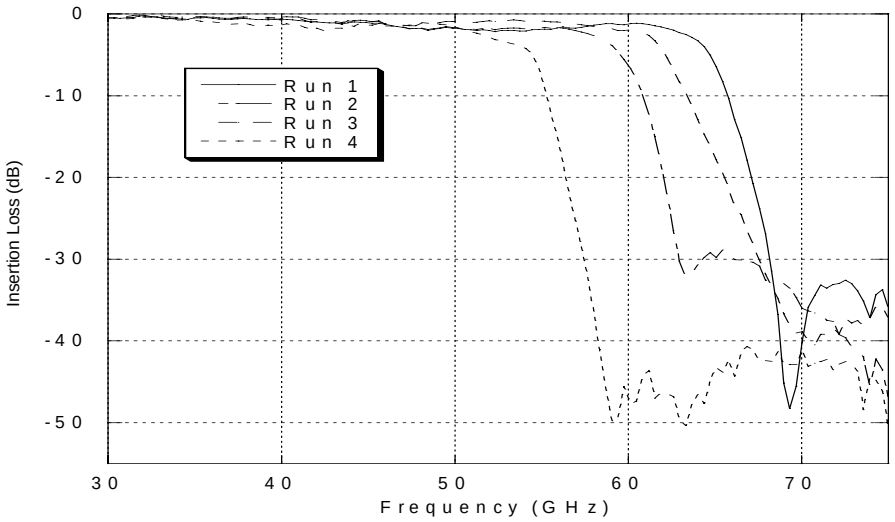


Figure 29. Measured insertion loss of low pass filter samples.

Table 13. Measured Data for Low Pass Filter

Run	Layout Parameters (μ m)					Electrical Parameters		
#	L1	L2	W	L	X	Cutoff Freq. (GHz)	Freq. @ 1st Pole	Atten. @ 1st Pole
1	400	500	250	425	375	63.8	69.3	-49.14
2	525	775	325	575	450	40.8	46.3	-24.412
3	525	600	300	425	425	52.08	59.06	-50.855
4	500	650	350	500	475	49.7	54.45	-43.83
5	375	550	275	450	350	53.15	63.3	-20.9
6	540	620	250	510	450	50.8	56.58	-44.81
7	430	550	270	600	350	58.17	63.32	-31.17
8	530	520	360	490	300	55.18	64.72	-55.96
9	440	460	380	500	330	58.03	70	-31
10	520	670	300	550	350	43.68	53.03	-18.16
11	380	630	290	530	430	47.48	56.57	-27.11
12	490	500	210	570	410	54.18	67.91	-47.7
13	510	570	240	430	440	52.86	60.83	-54.32
14	480	750	250	440	420	55.35	69.68	-40.77
15	470	770	340	550	500	39.39	46.27	-27.37
16	400	490	220	460	480	61.26	70	-39.21
17	370	590	390	580	390	48.21	59.77	-31.31
18	420	780	370	410	370	37.69	45.24	-25.93
19	350	710	320	400	470	41.42	49.85	-26.29
20	460	710	330	470	320	42.05	50.55	-23.22
21	400	650	280	480	390	58.76	70	-20.26

5.1.2. Neural Network Modeling

Neural networks were used to model the electrical response of the low-pass filters using measured data. The electrical response parameters were cutoff frequency,

attenuation, and frequency at the first pole. The neural network model exhibited a training error less than 5% for the cutoff frequency and frequency at the first attenuation pole. This accuracy is good, considering the error involved in measurement and parameter extraction at 40-70 GHz. The results of the neural network model are shown in Table 14. The prediction error for attenuation at the first pole was large, and this was likely due to errors involved in measurement of rejection losses of order of –50dB at high frequency and calibration errors.

Table 14. Neural Network Parameters For Low Pass Filter Modeling

Filter Parameter	**NN Structure**	**Learning rate (η)**	**Prediction Error**	
			RMSE	**% RMSE**
Cutoff Frequency	5-7-1	0.01	2.7	3.9
Frequency @ attenuation pole	5-7-1	0.01	7.9	4.8
Attenuation @ First attenuation pole	5-7-1	0.01	25.6	21

5.1.3. Neuro-Genetic Synthesis

The neural network models were used to design LTCC mm-wave low pass filters using the neuro-genetic approach. The genetic search parameters chosen are shown in Table VI. These parameters were chosen such that the algorithm converged to the desired optimal point with few iterations. Filter synthesis results are shown in Table 15. Attenuation at the first attenuation pole was not used for synthesis, as it had a large modeling error. The modeling error is large because of the randomness involved in acquiring very low values of attenuation of the order of -50 dB. The use of attenuation at the first pole as a targeted response during optimization would thus result in faulty layout prediction because of the large modeling error.

For the low pass filter, the measured results obtained from the synthesized filter were close to target values at 40 and 60 GHz. For a target cutoff frequency of 40 GHz and frequency at the first attenuation pole of 45 GHz, the neuro-genetically synthesized filter yield a cutoff frequency of 39.7 GHz and frequency at first attenuation of 47.5 GHz. This is quite good, considering the error involved in measurements and modeling-board to test-board fabrication variations. Thus, with a small number of experimental runs (16), a low pass filter was synthesized with precise cutoff frequency in the range of 35-65 GHz.

Table 15. Mm-Wave Low-Pass Filter Synthesis

		Cutoff Freq. (GHz)	**Freq@ atten. pole (GHz)**	**l_1, l_2, l_3, x_1, x_2 (μm)**
1	Target	40	45	-
	NN-GA	39.70	47.5	417, 760, 600, 375, 380
2	Target	60	65	-
	NN-GA	59	66	395, 500, 505, 300, 220

5.2. Bandpass Filter Synthesis

This section describes synthesis of bandpass filters for wireless LAN applications. Filters in the range of 5-6GHz range were synthesized. This range is designated for 802.11a and HIPERLAN/2 wireless LAN applications [60]. In this example, the neuro-genetic algorithm was applied in the iterative loop 1 (Figure 5) involving the CAD tool to minimize the time for filter synthesis.

5.2.1. Experimental Design and Data Acquisition

Filters are designed using a semi-lumped element approach with two pole-coupled resonators. The lumped element circuit topology of the bandpass filter is shown in Figure

30. The filter is realized by an innovative design with minimization of area using the folded structure shown in Figure 31. Single layer interdigitated microstrip structures act as feeding capacitors. Inductors operate at their self-resonating frequency and act as high-Q compact resonators. Capacitive coupling is achieved by broad side coupled microstrip line structure.

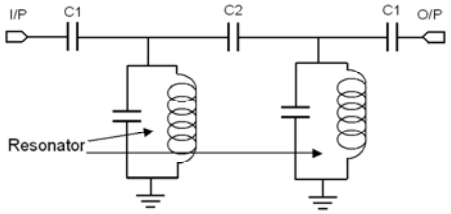


Figure 30. Topology of two-pole capacitively coupled resonator bandpass filter.

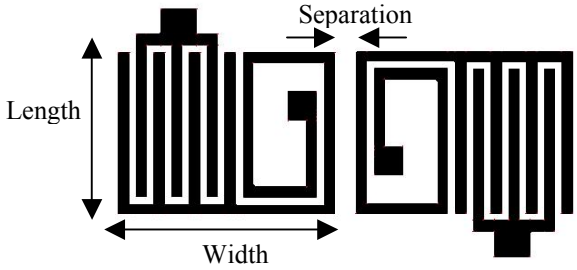


Figure 31. Microstrip line implementation of bandpass filter.

The relevant layout parameters are the length of the interdigitated capacitor and resonator (L), width of the resonator (W), and spacing between the resonators (S) (Figure 31). The bandpass filter is implemented on a 4 mil thick low-cost Rflex 3600 liquid crystal polymer (LCP) substrate (dielectric constant = 2.9, loss tangent = 0.002). The ranges for the three layout parameters were selected such that the insertion loss was 1.5 - 3 dB and fractional bandwidth was 4 - 12%. These design specifications are suitable for 802.11a and HIPERLAN/2 wireless LAN front-end applications. The ranges of layout parameters are shown in Table 16. The simulated insertion losses of sample filters are

shown in Figure 32. Latin hypercube sampling was used once again. The extracted simulation data is shown in Table 17.

Table 16. Range of Layout Parameters for Bandpass Filter

Layout Parameter	Low (mils)	High (mils)
Length of resonator (L)	40	47
Width of resonator (W)	30	35
Separation between resonators (S)	3	5

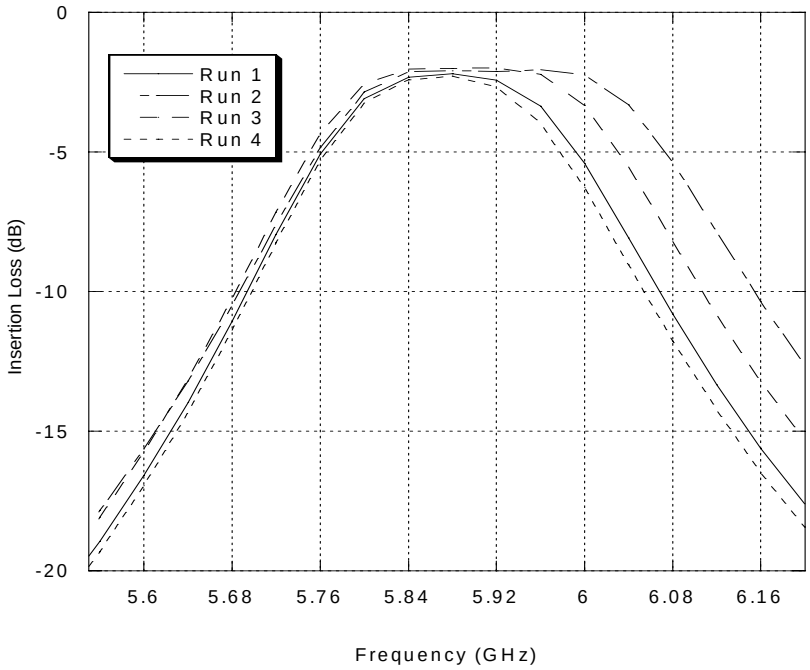


Figure 32. Simulated insertion loss of bandpass filter samples.

Table 17. Extracted Data for Bandpass Filter

Run	Layout Parameters (μ m)			Electrical Parameters		
#	Length	Width	Separation	Insertion Loss (dB)	Bandwidth (MHz)	Center Freq. (GHz)
1	47.5	32.5	3.5	2	240	5.11
2	42	31.5	3.5	2.05	280	5.64
3	47	31	4.5	2.17	230	5.19
4	42.5	30	5	2.57	210	5.68
5	46.5	33	4	2.05	250	5.16
6	39.5	32.5	4	2.2	240	5.88
7	45	30.5	3	2.05	330	5.36
8	46	31.5	3.5	1.99	280	5.3
9	44.5	34.5	3.5	2.06	270	5.3
10	44	34.5	4.5	2.34	220	5.32
11	40.5	30.5	3	2.08	320	5.82
12	39	32	5	2.8	200	5.94
13	41.5	34.5	4.5	2.4	200	5.58
14	38	34	4	2.3	220	5.98
15	43.5	33.5	4.5	2.29	220	5.42
16	40.5	33	4	2.18	240	5.74
17	40.5	32	4	2.16	240	5.78
18	44	30.5	3	2	320	5.5
19	46	34.5	3.5	2.04	270	5.16
20	42	31	4.5	2.28	220	5.68

5.2.2. Neural Network Modeling

Although theoretical analysis of this particular topology is provided in detail in [61] based on a lumped element approach, this modified compact implementation is much more complex to analyze and model accurately. The main issue is the electromagnetic

interaction between the interdigitated capacitor and resonator because of the small physical separation. The capacitive coupling can be modeled as a series capacitance (for small gaps) and additional negative shunt capacitances (for large gaps). Optimization of all layout parameters with existing modeling techniques requires extensive effort. Interactive optimization with EM tools is time consuming. Therefore, this filter example is suitable for neuro-genetic design.

Neural networks are used to model the center frequency, 3 dB bandwidth and minimum insertion loss as a function of the three layout parameters. The neural network structure and parameters (Table 18) were optimized to obtain greater accuracy with minimal training. The average prediction error obtained was less than 3%. Thus the neural network was effective in modeling the bandpass filter response to the layout parameters. This accuracy is good and the RMSE error is less than the case of low pass filter example because the simulated data is used for modeling. Generally, the simulated data is not noisy and has less random errors as compared to the measured data.

Table 18. Neural Network Parameters for Bandpass Filter

Filter Parameter	**NN Structure**	**Learning rate (η)**	**Prediction Error**	
			RMSE	**% RMSE**
Center Frequency	3-5-1	0.1	0.029	0.74
Insertion Loss	3-5-1	0.1	0.033	1.11
Bandwidth	3-5-1	0.1	13.19	4.1

5.2.3. Sensitivity Analysis and Response Surface Modeling

Sensitivity analysis was performed using the neural network models. These results (Figure 33) reveal that the center frequency depends primarily on the length and width of the resonator, while the insertion loss and bandwidth are most sensitive to the separation

between the resonators. Physically, resonator length and width denote the effective length of the microstrip line, and their increase should cause a decrease in center frequency. The separation between the resonators determines the coupling capacitance. Increased separation decreases the coupling capacitance, and hence, bandwidth decreases. Overall, the sensitivity results reflect the trends expected from the physics of the filter topology accurately.

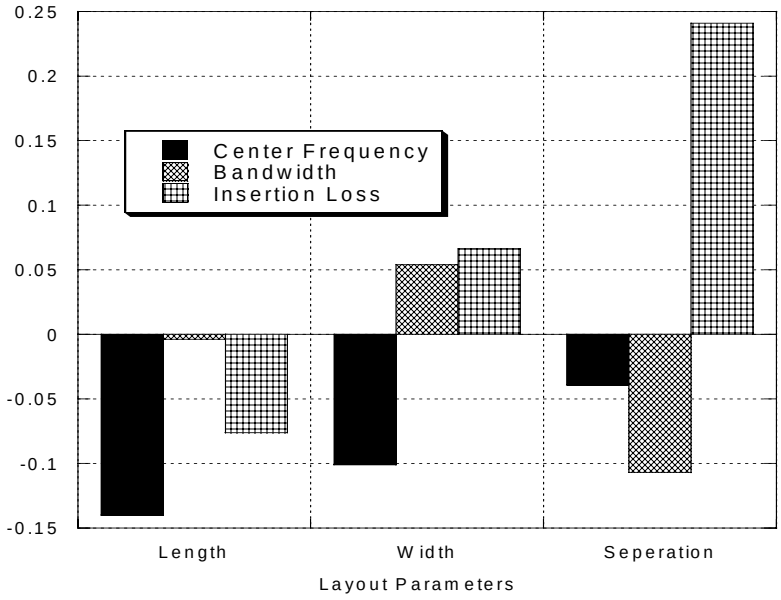


Figure 33. Sensitivity analysis of bandpass filter.

Response surfaces (Figures 34-35) for the performance parameters were generated as a function of the two most sensitive layout parameters at the mean value of the remaining parameter. Increasing the length and width of the resonator increases the effective length of the microstrip filter line and hence, decreases the resonance or center frequency. Increasing the separation between the resonators decreases coupling capacitance, and hence, bandwidth decreases.

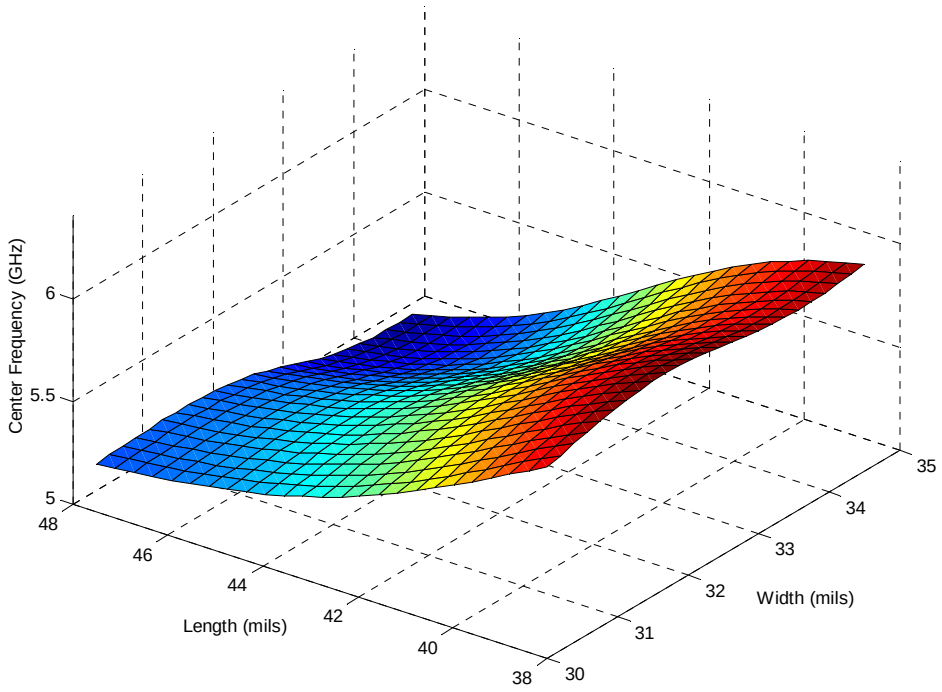


Figure 34. Center frequency vs. layout of bandpass filter.

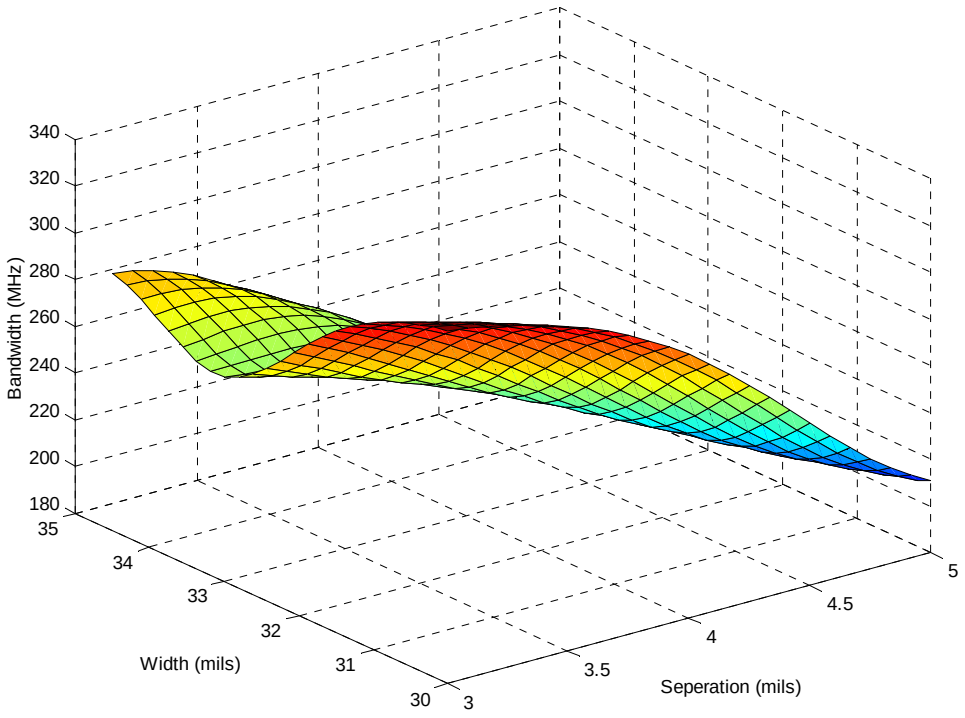


Figure 35. Bandwidth vs. layout of bandpass filter.

5.2.4. Filter Synthesis with Equal Priority

The IEEE and the European ETSI organization have determined their respective standards for the 5 GHz band: IEEE 802.11a [62] and HIPERLAN/2 [63]. The targeted values for 802.11a are an insertion loss of 2 dB, bandwidth of 200 MHz, and center frequency of 5.2 GHz. However, for HIPERLAN2, these are 2 dB, 255 MHz and 5.6 GHz respectively. The results of neuro-genetic bandpass filter synthesis for these standards are shown in Table 19.

Table 19. Neuro-Genetic Design of Bandpass Filters with Equal Priority

#		**Insertion Loss (dB)**	**Bandwidth (MHz)**	**Center Freq. (GHz)**	**L, W, S (Mils)**
1	Weight	100	0	0	-
	Target	2	NA	NA	-
	NN-GA	2.08	290	5.12	47.5, 32.3, 3.3
2	Weight	0	100	0	-
	Target	NA	200	NA	-
	NN-GA	2.44	200	5.44	43.2, 33.4, 4.8
3	Weight	0	0	100	-
	Target	NA	NA	5.2	-
	NN-GA	2.02	250	5.18	47.2, 30.8, 4
4	Weight	100	100	100	-
	Target	2	200	5.2	-
	NN-GA	2.04	240	5.2	46.5, 32.2, 3.9
5	Weight	100	100	100	-
	Target	2	255	5.6	-
	NN-GA	2.03	260	5.58	42.5, 32, 3.58

The first three optimization results reflect single parameter optimization to obtain an insertion loss of 2 dB, a bandwidth of 200 MHz, and a center frequency of 5.2 GHz,

respectively. It can be seen that single parameter optimization is not sufficient. For filter synthesis with an insertion loss of 2 dB, the bandwidth and center frequency are not close to the values of 200MHz and 5.2 GHz. Obtaining a bandwidth of 200 MHz by single parameter optimization (trial 3) results in a high value of insertion loss and center frequency. For trial 4, although the insertion loss and center frequency are close to the desired values, the bandwidth is not close to 200 MHz. In trials 4 and 5, multi-parameter synthesis was performed with all three electrical response assigned equal priority. For trial 5, all three synthesized values are close to targets. However, for trial 4, the value of bandwidth is not close to targeted vale of 200 MHz. This indicates that to obtain a narrow bandwidth of 200 MHz, together with an insertion loss of 2 dB and center frequency of 5.2 GHz, the weight assignments during optimization have to be adjusted to obtain precise target values.

5.2.5. Filter Synthesis with Priority to Account for Tradeoffs

The priority during filter design is provided by weight assignment. A higher weight assigned to a parameter indicates greater priority than a parameter with lower weight assignment. To achieve 2 dB insertion loss, 200 MHz bandwidth, and 5.2 GHz center frequency, several weight combinations were investigated (Table 20). In trial 1, the highest weight (100) was given to bandwidth with center frequency and insertion loss weighted low (5). This resulted in meeting the bandwidth specification of 200 MHz, but the center frequency and bandwidth did not meet the targeted specifications. In subsequent trials, the weights of the center frequency and insertion loss were increased and adjusted to a level that did not affect the bandwidth and provided the best

compromise. Finally, in trial 4, the insertion loss, bandwidth and center frequency were given weights of 50, 100 and 75, respectively. This provided the best working solution within the given design constraints. Thus, it can be concluded that the priority scheme with weight assignment is an effective strategy for multi-parameter design involving tradeoffs.

Table 20. Neuro-Genetic Design of Bandpass Filters with Variable Priority

#		**Insertion Loss (dB)**	**Bandwidth (MHz)**	**Center Freq. (GHz)**	**L, W, S (Mils)**
1	Weight	5	100	5	-
	Target	2	200	5.2	-
	NN-GA	2.46	200	5.4	43.5, 33.7, 4.8
2	Weight	50	100	50	-
	Target	2	200	5.2	-
	NN-GA	2.08	230	5.21	46.2, 32.3, 4.1
3	Weight	5	100	50	-
	Target	2	200	5.2	-
	NN-GA	2.52	180	5.22	45.3, 34.4, 5
4	Weight	50	100	75	-
	Target	2	200	5.2	-
	NN-GA	2.15	220	5.17	47.1,31.3, 4.5

5.3. Computational Cost Comparisons in Filter Design

To illustrate the computational advantage of the proposed method, the approximate time required to synthesize a bandpass filter using an EM simulator and neuro-genetic method were compared. A method of moments (MOM) based 2-D simulator was used [64]. The neuro-genetic and EM simulations were run on Pentium III, 996 MHz processor with 256 MB of RAM. As shown in Table 21, the neuro-genetic approach

consumes significantly less time (90% less) compared to the EM simulator. A full wave 3-D simulator would consume even more time. Even during neuro-genetic design much, of the time is consumed in data acquisition by EM simulator.

Table 21. Computational Cost Comparison for Filter Design

Design Step	**Neuro-Genetic**	**MOM**
Data Extraction	16 x 1800 sec	-
Training/ Modeling	3 x 100 sec	-
Optimization	20 sec	150 x 1800
Total Time	29120 sec	270000

The space mapping technique for optimization proposed in [65] uses coarse empirical functions or equivalent circuit models, which are computationally very efficient. However, it has been proved that neural networks are more accurate than other empirical models [66]. Furthermore, space mapping methods typically use the gradient descent approach. Genetic algorithms are more efficient in nonlinear multi-parameter search. Thus, the neuro-genetic method provides greater accuracy while lowering the cost of microwave filter design over existing techniques.

5.4. Summary

A neural network and genetic algorithm based methodology has been demonstrated for modeling, analysis and synthesis for microwave filters. The proposed method has been used during the CAD or post-fabrication stage to fine tune the design to meet precise electrical characteristics. The method has been used for synthesis of mm wave low pass filters and wireless LAN bandpass filters with high accuracy. The neuro-genetic approach results in significant time reduction over existing methods. The priority scheme

has been used effectively to account for the tradeoffs among various filter design parameters and obtain the best available design within given constraints. The generic nature of the methodology suggest possible extension to design active microwave circuits like low noise amplifiers, voltage controlled oscillators, etc., and passive components like diplexers and antennas.

CHAPTER 6

Design Centering and Yield Enhancement

There is increasing demand for enhanced system manufacturability in the microwave industry to increase yield and reduce cost. Despite advances in equipment and fabrication techniques, random fluctuations in IC manufacturing facilities still exist. The uncontrollable stochastic nature of fabrication processes has a direct impact on production yield. Therefore, yield analysis and optimization methods, which take into account manufacturing tolerances, model uncertainties, variations in the process parameters, etc., have become indispensable components of microwave circuit design [67]-[69]. Moreover, statistical circuit optimization has become imperative prior to high-volume manufacturing.

The yield maximization problem, also known as the design centering problem [70], essentially focuses on obtaining nominal values and tolerances of design parameters (process or layout) that lead to a greater number of circuits meeting a desired set of electrical specifications. The cost of obtaining an accurate yield estimate is usually high, since a large number of simulations are required. There are typically a large number of variables to consider, and hence, the dimensionality of the optimization problem is also high. Moreover, the design variable space is irregular, ill-behaved, and difficult to track analytically.

A number of methods have been proposed in the literature in the area of statistical circuit design [71]. These methods generally fall into two categories: Monte Carlo and geometric [72]. Monte Carlo methods are more general and do not require any

assumption about the form of the input distribution, nor about the shape of the circuit acceptability region [73]. The sample size required for yield estimation is independent of the problem dimension. However, Monte Carlo methods are computationally intensive and require large numbers of simulations. Moreover, optimization in the Monte Carlo methods must deal with an often ill-behaved yield function, and most optimization methods require derivative information about the objective function and continuity of the search space. On the other hand, geometrical methods transform the statistical optimization problem into a deterministic one. They do not have to deal with ill-behaved yield functions, since yield is not used directly as an objective. However, most geometrical methods assume some approximation for the feasibility region, such as a hypersphere or ellipsoid. Geometrical methods like the simplicial approximation [74] assume convexity of acceptability region, and a large number of simplices are required as dimension of the problem increases.

In this chapter, a novel neuro-genetic design centering methodology is presented. An accurate neural network model is used for the yield calculation using Monte Carlo methods. This method does not make any assumptions regarding the acceptability region or input distributions. A genetic algorithm is used for yield optimization since such algorithms are capable of searching efficiently through large nonlinear and irregular shapes. GAs do not require any derivative information about the yield function or convexity of the acceptability region for optimization. They only require the objective function value (yield value), thus making them an ideal choice for yield optimization and design centering. In subsequent sections, the proposed method is presented and applied for design centering of SiGe heterojunction transistors and 30 GHz voltage controlled

oscillators. It has also been shown how the proposed methodology can be extended for circuit, package and system level co-design. Thus the proposed methodology can be used to develop a methodology that optimized device, circuit, package, and board level parameters simultaneously and produces an overall optimized design.

6.1 Design Centering Problem

The objective of the design centering or yield maximization problem is to maximize the number of fabricated microwave circuits whose performance meets a set of desired specifications. The parametric yield of a device or circuit is defined as the portion of the manufactured devices that satisfies a set of acceptability constraints defined by the user. The parametric yield of a device Y, can be expressed as

$$Y = \int_{a_y} f_y(y)\, dy \tag{17}$$

where y is vector of device characteristics or response of interest (e.g., cutoff frequency, gain, etc.); $f_y(\cdot)$ is joint probability density function (*jpdf*) of y; and a_y is the output acceptability region in the y-space defined by acceptability constraints, $y_L \le y \le y_U$, i.e., $a_y = \{y | y_L \le y_U\}$. In general, the vector y is composed of implicit functions of process or design variable vector x. We now define the yield maximization problem as

$$\begin{aligned} &\max_x \; Y \\ &subject\ to\ x \in D \end{aligned} \tag{18}$$

where D is the region which defines the allowable values for variable in x vector.

In general, the $f_y(\cdot)$ cannot be easily evaluated in (17) because it is an implicit function for x whose form is not known a priori. The relation between nominal values of

x and electrical response y often requires numerical simulation. There have been attempts in the past to use regression models or neural network models [75] to map these relationships in order to avoid the computational costs inherent in simulation. After modeling, yield has been maximized using optimization methods like gradient descent or by inscribing hyper spheres with largest dimension [76]. Both the approaches are limited in scope due to the nonlinear nature of the yield function and irregular and indeterminate shape of the feasibility region.

6.2 Neuro-Genetic Design Centering

In the proposed design centering methodology, neural network models developed from either experimental or simulation data are used for mapping input and output parameters of the devices. These models are used as an alternate and efficient way to calculate yield, rather than performing a large number of time-consuming Monte Carlo trials by process or circuit simulators. Once the yield is determined, design centering is performed using genetic algorithms, since they are efficient for nonlinear search and do not require derivative information about the yield function. The neuro-genetic design centering methodology thus has two stages. Stage 1 is the parametric yield estimation stage wherein yield is estimated by performing Monte Carlo simulations using neural network models. In the second stage, the parametric yield estimator is coupled with genetic algorithms to facilitate the search for the design center that provides the greatest yield.

6.2.1. Parametric Yield Estimation

The parametric yield estimation stage begins with a random sample generator that uses Monte Carlo runs to generate a large number of input vectors based on the mean, variance, and distribution of the input variables. Examples of input variables for a MOSFET could be gate length, channel dose, oxide thickness, etc., or for an HBT, emitter length or emitter, base, and collector doping. Various other sampling methods discussed in [77] can be used to reduce number of runs. Since neural network models are used for the output value calculation, the use of Monte Carlo sampling is not prohibitive. The outputs calculated might be transconductance, saturation, or leakage current for MOSFETs. Similarly, for a SiGe HBT, these might be transistor gain, cutoff frequency, or breakdown voltage. Once the output values are determined for each run, the yield is determined using a yield calculator. Parametric yield is calculated based on the upper and lower specifications for each output or electrical response. The yield for each an individual output is:

$$\begin{aligned} Y_1 &= \left\{ y \middle| y_{1\min} \le y_1 \le y_{1\max} \right\} \\ Y_2 &= \left\{ y \middle| y_{2\min} \le y_2 \le y_{2\max} \right\} \\ &\vdots \\ Y_i &= \left\{ y \middle| y_{i\min} \le y_i \le y_{i\max} \right\} \\ &\vdots \\ Y_n &= \left\{ y \middle| y_{n\min} \le y_n \le y_{n\max} \right\} \end{aligned} \tag{19}$$

where Y_i is the partial yield of ith output and Y_{imin} and Y_{imax} are lower and upper specification respectively and n is the number of output values. The total yield of the device is:

$$Y = Y_1 \cap Y_2 .... \cap Y_i ... \cap Y_n \tag{20}$$

In this method, fixed mean values, variances, and distribution types for each process variable are provided to the parametric yield calculator along with desired specification limits of output of electrical response. This stage then provides the value of yield for the current mean and variance of input variables. The flow chart for the stage 1 (parametric yield estimation) is shown in Figure 36.

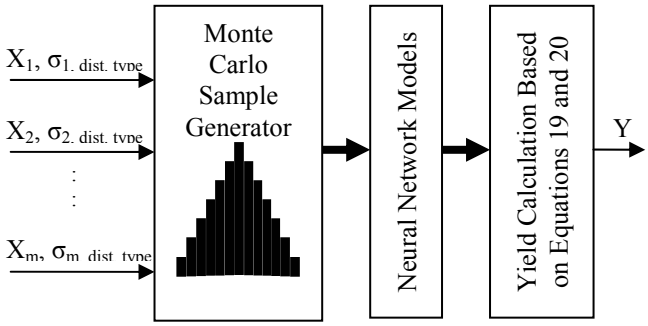


Figure 36. Parametric yield estimation.

6.2.2. Genetic Design Centering

In this stage, the parametric yield estimator is coupled with a genetic scheme for design centering. The values obtained from the parametric yield estimator are used in conjunction with genetic algorithms to determine the means and variances of the input parameters that result in the maximum parametric yield. We assume that the distribution of the input variable is independent of its mean and variance. We also assume that input parameters are statistically independent and variances are independent of means. This method does not require convexity of design space, as is the case with most geometrical methods [78].

The flow diagram for neuro-genetic design centering is shown in Figure 37. The genetic algorithm starts with an initial population (P) of means and variances of input parameters. The parametric yield estimator calculates the yield for each member of

population. If the yield of any population exceeds the desired maximum yield, that sample is deemed the design center, and the algorithms stops. If, however, the yield values are below a specified value, the population of means and variances is provided to the genetic algorithm block along with the corresponding parametric yield values. The algorithm then performs genetic manipulations to obtain a new population of means and variances. During genetic manipulation, the samples with higher yield are assigned greater "fitness" values, leading to a higher probability of survival in the new population set. The process is continued iteratively until a suitable design center.

This method is capable of design centering with constant or variable means and variances. For a case with constant variances, the population manipulated will include only the mean vales of input parameters. On the other hand, variable means and variances would require manipulation of both parameters.

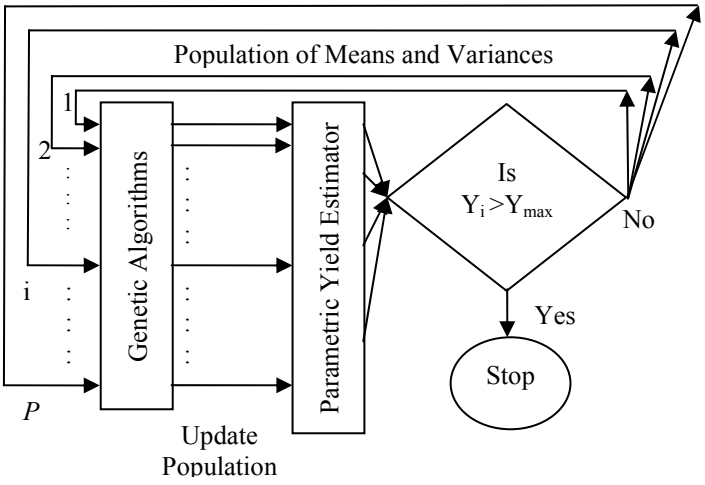


Figure 37. Neuro-genetic design centering.

6.3 Design Centering of Heterojunction Bipolar Transistor

In this section, the proposed method is used for design centering of SiGe heterojucntion bipolar transistors. A neural network model is developed mapping the key

structure and process parameters of SiGe HBT with the electrical responses. Then the method is used to obtain the mean values of the input parameters that would give the highest yield.

6.3.1. SiGe Heterojunction Bipolar Transistor

The first functional SiGe HBT devise was demonstrated in 1987 [79]. From the RF viewpoint, state of art SiGe HBTs offer frequency response, noise figure, and linearity comparable to current generation III-V devices, and better than both Si-BJTs and Si-CMOS (even highly scaled CMOS) [80]. The compatibility of SiGe HBT fabrication with fairly mature traditional silicon fabrication makes it a very low-cost alternative to compound semiconductor devices for high performance RF applications. Therefore, there has been rapid increase in research and development activities of SiGe devices. Most of the research is focused on low-cost and reliable fabrication processes for these devices, since successful commercialization of SiGe HBT devices high yield is very important.

6.3.2. Experimental Design and Parameter Extraction

The schematic for a 0.15-μm, n-p-n $Si_{0.8}Ge_{0.2}$ HBT is shown in Figure 38 [81]. The four key structural and doping parameters are shown in Table 22, along with their variances and distributions. The variances are assumed to be constant and independent of the means. The choice of these values is based on the concentration profile curve for the HBT devise shown in Figure 39 [82].

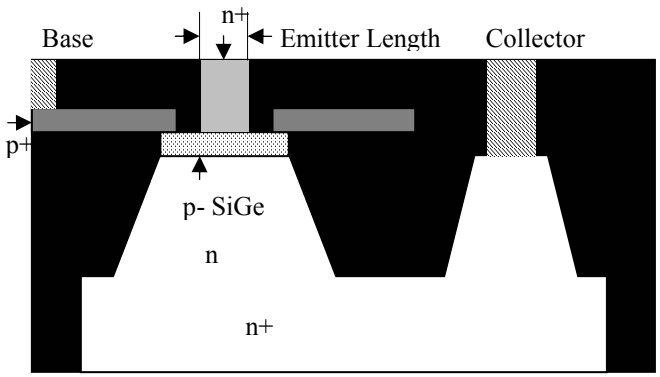


Figure38. Schematic of 0.15-µm SiGe HBT.

Table 22. SiGe HBT Parameters

Input Parameter	Range for Mean		Distribution Type	Standard Deviation
	Low	High		
Emitter Length (µm)	0.1	0.16	Normal	0.006
Collector Doping (avg)	5e16	5e17	Normal	4.5e16
Base Doping (avg)	1e19	1e20	Normal	1e19
Emitter Doping (avg)	1e19	1e20	Normal	1e19

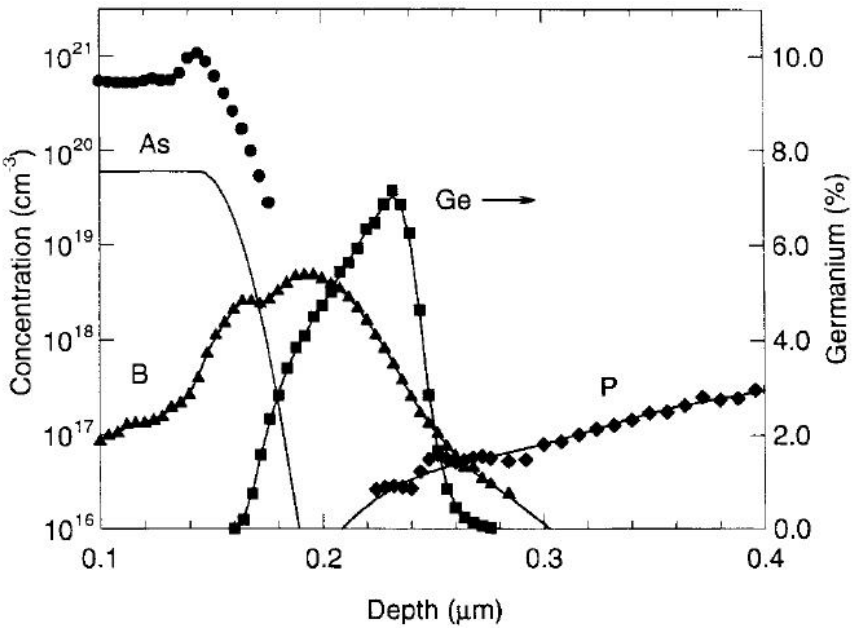


Figure 39. SIMS profile of a representative SiGe HBT.

The electrical performance (i.e., output) parameters under consideration are the maximum DC gain (β) and the peak cutoff frequency (f_T) of the HBT. In order to extract these parameters for various device input combinations, the Synopsis ISE TCAD^{TM} device simulator from was used [83]. Two-dimensional device simulations were performed. Latin hyper cube sampling was used for experimental design. The gain of the HBT device was obtained from Gummel plot simulations (Figure 40). The cutoff frequency was defined as the frequency at unity current gain (i.e., f_T occurs when $|h_{21}|$=1). The peak cutoff frequency for each run was obtained from unit gain frequency vs. the base voltage plot (Figure 41). The data obtained from 2-D SiGe HBT device simulations are shown in Table 23.

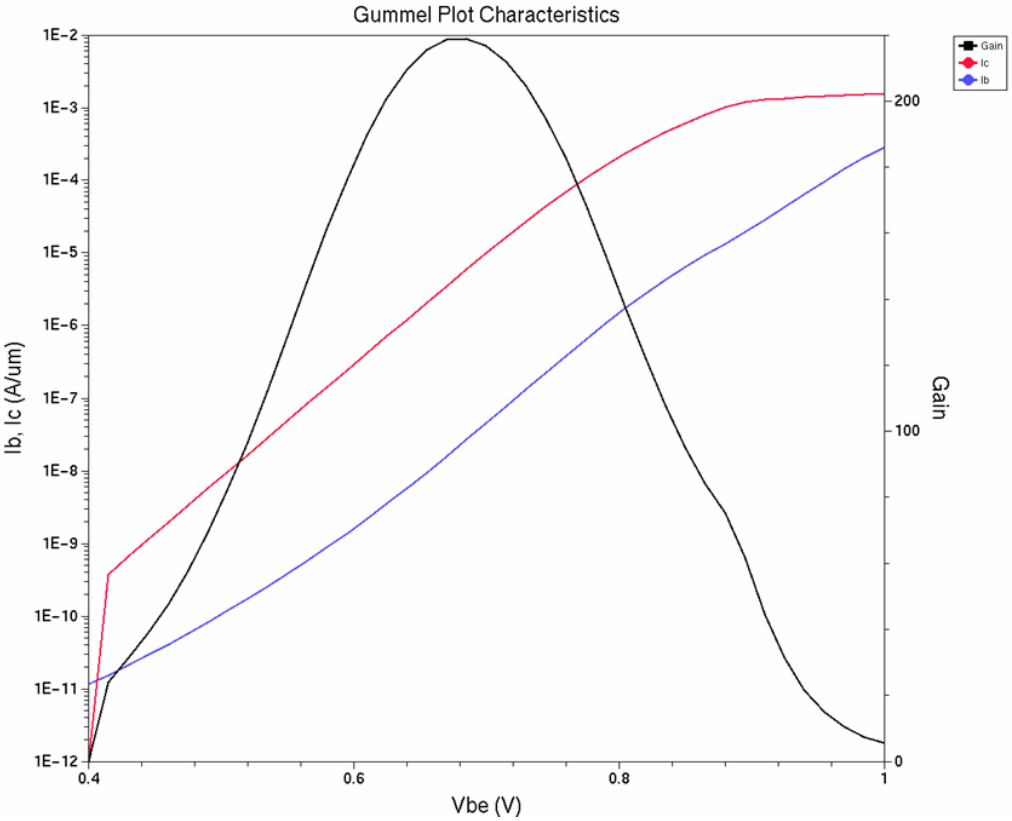


Figure 40. Gummel plot for HBT gain.

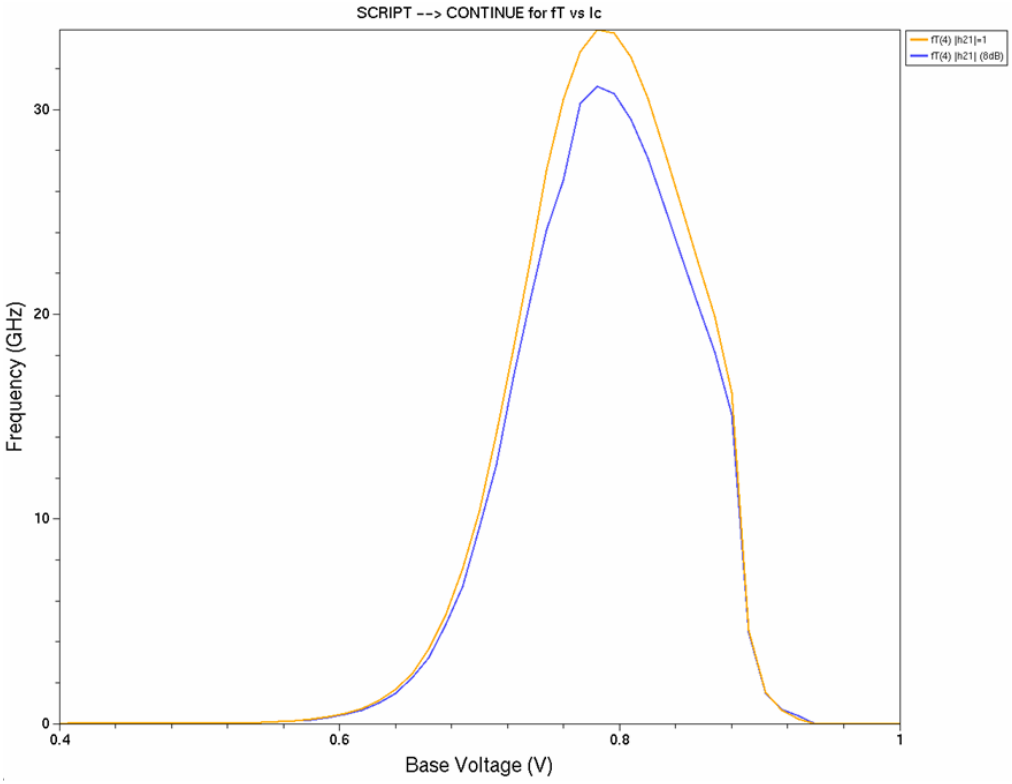


Figure 41. Unit current gain frequency (f_T) vs. base voltage for V_{cb} = 0.5 V.

Table 23. SiGe HBT Device Simulation data

#	Collector Doping (avg)	Base Doping (avg)	Emitter Doping (avg)	Emitter Length (μm)	β_{max}	Peak f_T (GHz)
1	5.00e+16	1.00e+19	1.00e+19	0.1	103.59	22.85
2	5.00e+16	1.00e+19	1.00e+20	0.16	93.43	26.98
3	5.00e+16	1.00e+20	1.00e+19	0.16	107.85	24.33
4	5.00e+16	1.00e+20	1.00e+20	0.1	90.5	22.53
5	5.00e+17	1.00e+19	1.00e+19	0.16	249.6	34.31
6	5.00e+17	1.00e+19	1.00e+20	0.1	197.96	30.79
7	5.00e+17	1.00e+20	1.00e+19	0.1	222.39	31.04
8	5.00e+17	1.00e+20	1.00e+20	0.16	218.93	33.91
9	2.75e+17	5.50e+19	5.50e+19	0.13	129.75	27.31
10	4.30e+17	7.90e+19	7.70e+19	0.12	169.82	29.88
11	5.70e+16	9.10e+19	5.20e+19	0.14	97.87	24.04
12	3.30e+17	1.60e+19	2.20e+19	0.15	172.7	31.18
13	1.10e+16	9.80e+19	4.40e+19	0.15	92.04	26.25
14	2.70e+16	8.50e+19	3.00e+19	0.15	96.73	22.9
15	2.00e+17	5.60e+19	3.40e+19	0.1	120.69	25.91
16	3.00e+17	2.70e+19	6.60e+19	0.11	136.49	27.89
17	2.40e+17	7.40e+19	8.70e+19	0.12	124.32	26.9
18	9.30e+16	6.70e+19	6.30e+19	0.12	98.57	24.17
19	4.90e+17	2.80e+19	1.10e+19	0.14	238.31	33.06
20	2.80e+17	1.10e+19	8.30e+19	0.13	123.64	27.44
21	3.70e+17	7.00e+19	9.60e+19	0.11	155.1	28.91
22	4.40e+17	4.20e+19	5.70e+19	0.14	191.78	32.01
23	1.30e+17	5.20e+19	4.60e+19	0.16	112.1	26.58
24	1.80e+16	4.80e+19	4.10e+19	0.15	93.71	22.36
25	3.90e+16	3.60e+19	2.80e+19	0.1	101.06	22.42
26	3.50e+16	4.10e+19	9.20e+19	0.13	87.83	21.85
27	2.10e+17	2.00e+19	1.60e+19	0.11	132.86	26.64
28	1.50e+17	6.10e+19	7.20e+19	0.11	106.13	25.17
29	4.70e+17	9.00e+19	8.10e+19	0.13	177.32	30.19
30	1.00e+17	1.00e+19	2.50e+19	0.15	117.42	26.38
31	2.00e+17	2.00e+19	4.50e+19	0.11	120.05	26.12
32	3.00e+17	3.00e+19	7.50e+19	0.15	140.82	30.3
33	4.00e+17	4.00e+19	3.50e+19	0.13	166.73	29.23
34	6.00e+16	5.00e+19	5.00e+19	0.14	98.8	24.15
35	7.00e+16	6.00e+19	8.50e+19	0.12	93.41	23.42
36	8.00e+16	7.00e+19	6.00e+19	0.11	97.49	23.7
37	9.00e+16	8.00e+19	9.00e+19	0.15	101.94	25.6
38	1.50e+17	9.20e+19	1.00e+20	0.15	110.17	26.96
39	1.00E+17	1.00E+19	1.00E+20	0.15	102.13	25.96

6.3.3. Neural Network Modeling

The 2-D device simulation data was used for neural network modeling to map device structure and doping parameters with maximum gain and peak cutoff frequency. Seventy-five percent of data was used for training, and 25% was used for testing. Individual neural networks were derived for each performance parameter to attain greater accuracy. The results are shown in Table 24. The network structure and learning parameters were optimized to obtain high accuracy with minimal training. The prediction errors of the models were less than 3%.

Table 24. Neural Network Parameters for HBT

Output Parameter	**NN Structure**	**η**	**Prediction Error**	
			RMSE	**%RMSE**
Maximum gain (β)	4-7-1	0.01	6.17	2.65
Peak Cutoff Frequency (f_T)	4-7-1	0.01	0.75	1.89

6.3.4. Design Centering

Design centering for the HBTs involved manipulation of the mean values only, as standard deviations were assumed to be constant and independent of the mean. The specification limits for the maximum gain and peak cutoff frequency were defined as:

$$\begin{aligned} 125 \le \beta_{\max} \le 175 \\ f_T \ge 30\ GHz \end{aligned} \tag{21}$$

A high value of peak cutoff frequency is required for high frequency device operations and superior noise performance. The maximum gain is generally specified by the application. Neuro-genetic design centering resulted in yield enhancement from 25%

to 75% after 115 iterations (Figure 42). The results of design centering are summarized in Table 25.

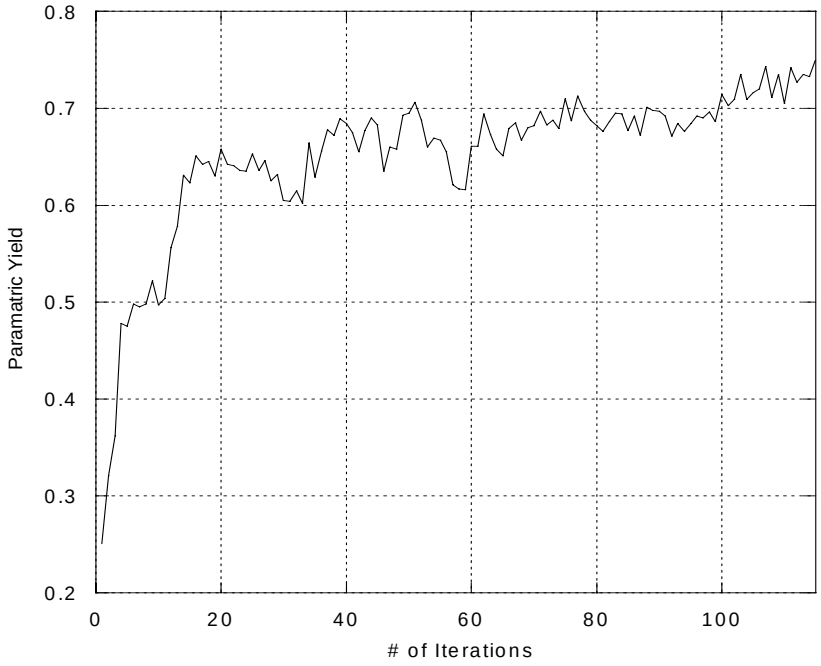


Figure 42. Parametric yield of HBT vs. # of iterations.

Table 25. HBT Design Centering

Input Parameters				
Parameters	**Initial Values (Yield =25%)**		**Final Values (Yield =75%)**	
	Mean	Std	Mean	Std
Emitter Length	0.13	0.006	0.15	0.006
Collector Doping	3.5e17	4.5e16	3.5e17	4.5e16
Base Doping	5.9e19	1e19	4.7e19	1e19
Emitter Doping	8e19	1e19	8.7e19	1e19
Output Parameters				
Parameters	**Initial Values (Yield =25%)**		**Final Values (Yield =75%)**	
	Mean	Std	Mean	Std
β_{max}	153.8	13.5	29.5	1.06
f_T	156.07	13.5	31.07	1.16

6.3.5. Yield Sensitivity Histograms

The results of design centering can also be illustrated using yield sensitivity histograms. Figures 43 and 44 show a comparison of peak cutoff frequency before and after design centering, respectively. As shown in Figure 43, a large proportion of the devices have an f_T below 30GHz before design centering, resulting in low parametric yield. However, after design centering (Figure 44), parametric yield is improved substantially. Similar results can be observed from the histogram of maximum gain (Figures 45-46).

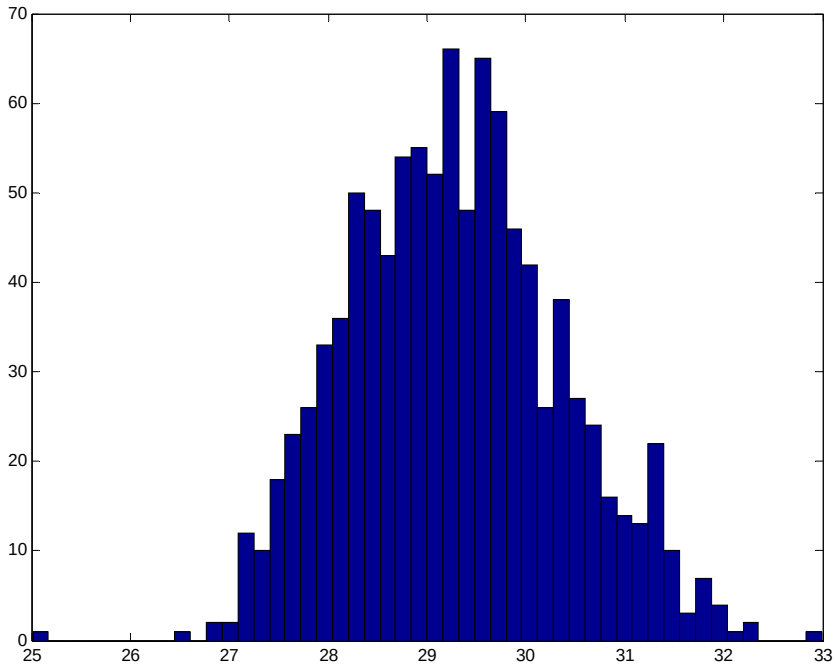


Figure 43. Yield histogram of peak cutoff frequency before design centering.

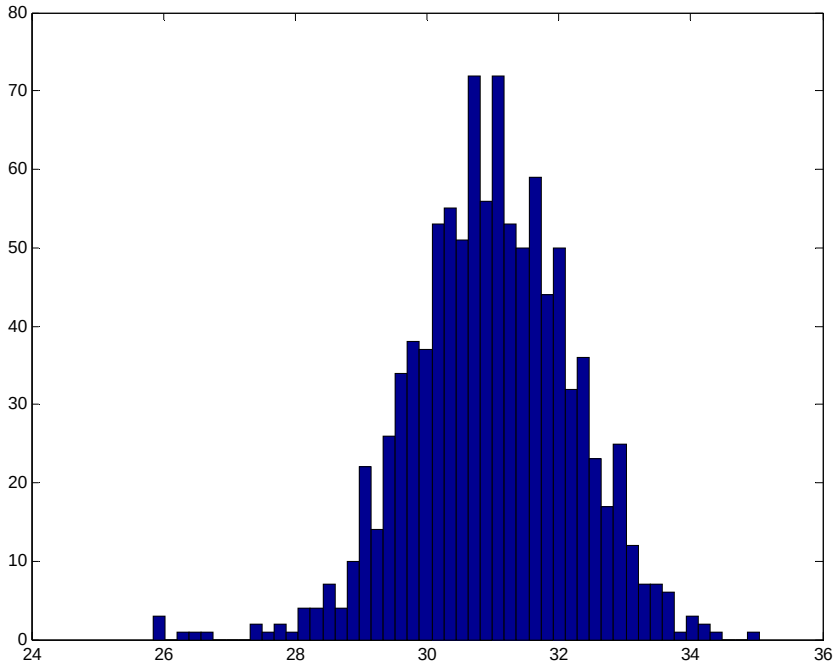


Figure 44. Yield histogram of peak cutoff frequency after design centering.

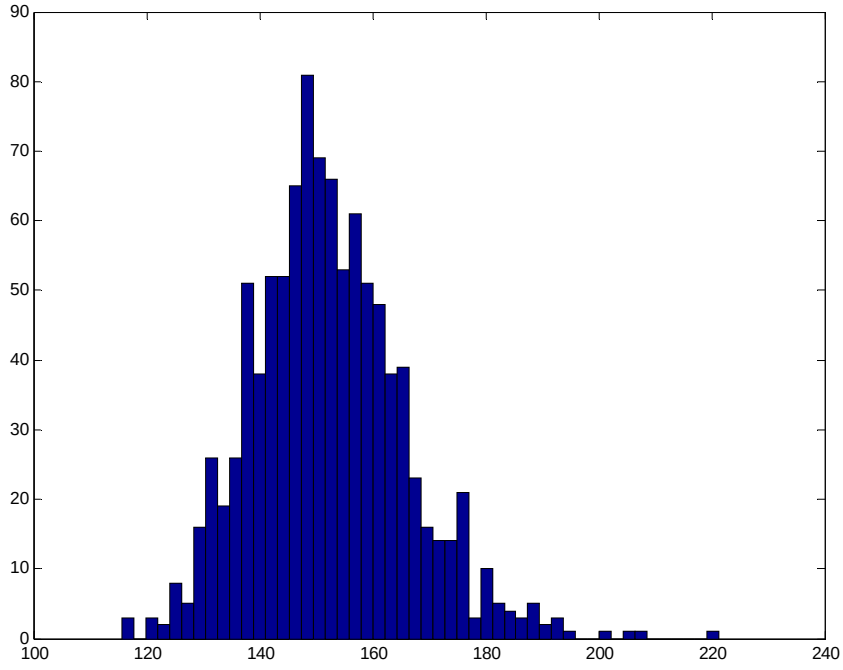


Figure 45. Yield histogram of maximum gain before design centering

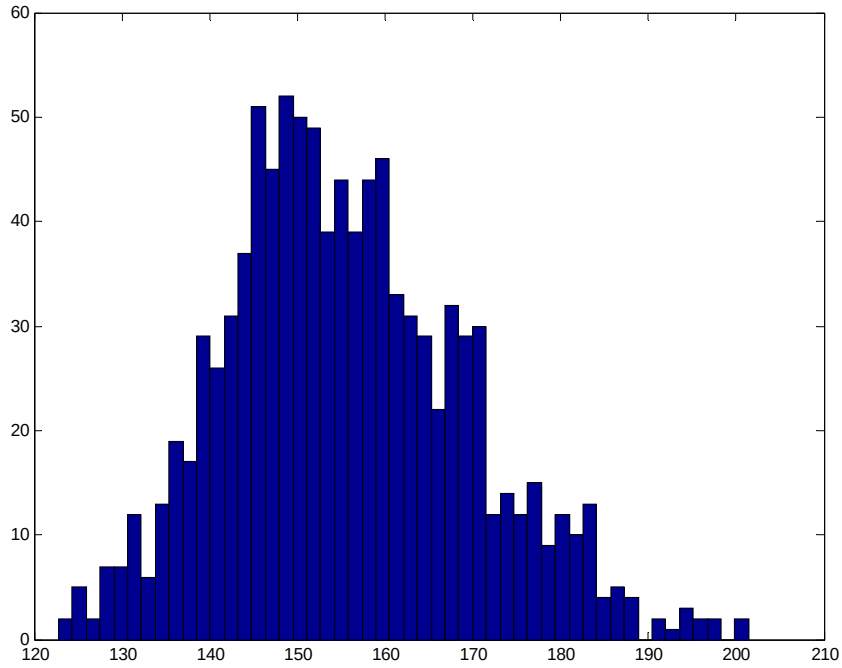


Figure 46. Yield histogram of maximum gain after design centering.

6.4 Methodology for Circuit, Package and System Co-design

Most of the tools in electronic design are limited at device, IC, package, and system levels. Therefore, the optimized designs obtained are optimized at each level. However, due to the complexity of modern systems, an overall optimization method is desired that takes device, IC, package and board level parameters into account. In this section the proposed method is used for optimization of a voltage-controlled oscillator (VCO) with package parameters included.

6.4.1. Voltage Controlled Oscillator Topology and Experimental Design

A 30 GHz VCO was designed using differential cross-coupled topology (Figure 47). NMOS buffers were used at the output stages for the required high to 50Ω impedance

conversion. Varactor diodes were used for varying the frequency with the applied tuning voltage. All the capacitors are the MIM type. The transistors in cross-coupled configurations were current-biased. The tuning voltage was varied between zero and the power supply voltage of 1 V. To account for packaging effects, inductances were added to the differential outputs. For analysis, the emitter lengths of SiGe HBT transistors, bias currents, anode dimensions for the varactor diodes, and package inductances were varied (Table 26). The standard deviation was chosen to be 5% of the range of variation of the mean. The value of inductance (L_{osc}) was chosen such that the center frequency at V_{tune} = 0.5 V was 30 GHz for each set of inputs. The electrical performance outputs were the tuning range, phase noise at 1 MHz offset, and fundamental power output. Experimental design was performed using Latin hypercube sampling and data is shown in Table 27.

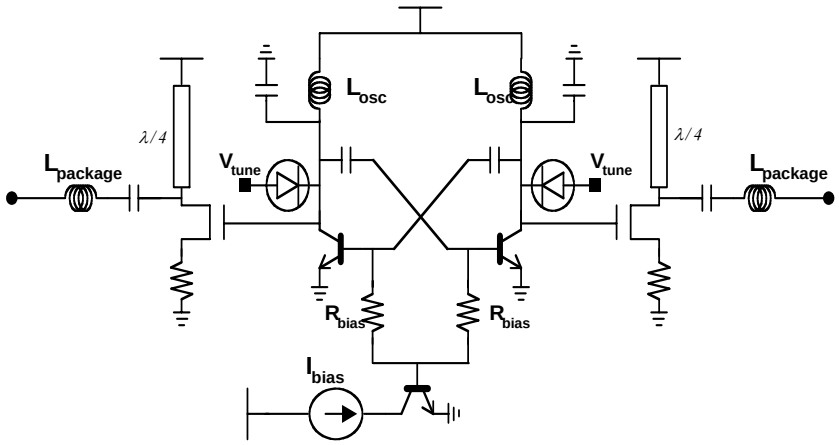


Figure 47. The topology of the cross-coupled VCO.

Table 26. VCO Input Parameters

Input Parameter	Range for Mean		Distribution type	Standard Deviation
	Low	High		
Emitter Length (μm)	2	10	Normal	0.4
Ibias (mA)	2	10	Normal	0.4
Cvardim (μm)	10	30	Normal	1
$L_{package}$ (pH)	50	100	Normal	2.5

Table 27. VCO Experimental data

#	Emitter Length (µm)	I_{bias} (mA)	Cvardim (µm)	$L_{package}$ (pH)	Tuning Range (GHz)	Phase Noise (dBc/Hz)	Output Power (µW)
1	7.2	3.7	24	83	1.94	-92.2	56.23
2	7.4	2.7	27	92	2.1	-91.2	51.28
3	3.1	4.5	19	50	1.97	-93.5	51.28
4	3.6	4.3	16	52	1.74	-91.2	51.28
5	6.2	8	23	55	1.99	-93.9	60.25
6	5.1	6.3	18	73	1.72	-94	61.80
7	6.8	2.2	13	89	1.26	-93.2	67.60
8	8.3	5.6	28	96	2.1	-92.7	58.88
9	5.3	2.9	17	79	1.58	-94.6	63.09
10	5.8	4.1	26	85	2.08	-95	63.09
11	2.7	7.1	27	94	2.57	-93.4	43.65
12	8.6	9.1	12	92	1.18	-90.5	61.65
13	3.4	3.4	14	100	1.6	-90.8	50.11
14	4.8	7.9	30	70	2.42	-94.6	54.95
15	9.5	3.1	20	64	1.69	-90.6	56.23
16	4.6	10	28	98	2.35	-94	54.95
17	7.9	8.4	11	88	1.12	-91.1	63.09
18	2.1	5.8	10	54	1.35	-91.2	41.68
19	2.9	5.4	14	61	1.63	-92.3	50.11
20	4.4	3.8	25	78	2.23	-91.8	50.11
21	4.1	8.8	23	60	2.1	-93.4	54.95
22	8.1	8.6	29	66	2.21	-93	57.54
23	6.7	9.5	18	75	1.66	-92.9	61.65
24	2.4	6.7	15	56	1.83	-92.1	44.66
25	5.5	7	16	68	1.57	-93.8	63.09
26	9.5	4.8	25	63	2	-91.7	61.65
27	6.3	2.3	22	87	1.92	-94.8	64.56
28	7.6	9.7	21	81	1.83	-92.6	60.25
29	9.8	5.2	20	58	1.69	-91.1	61.65
30	9.2	6	13	75	1.25	-90.6	63.09
31	8.7	7.3	21	70	1.79	-91.9	60.25
32	3.7	7.7	12	84	1.42	-91.7	57.54
33	4.5	7.5	18	80	1.68	-92.5	56.88
34	6.8	10	21	75	1.89	-92.5	57.41
35	7.7	4.2	25	57	1.94	-92.4	56.23
36	9	6.7	29	70	2.16	-92.2	58.88
37	5	6.6	17	95	1.71	-93.8	61.65
38	3.1	3.9	27	67	2.34	-94.2	47.86

6.4.2. Neural Network Modeling

Seventy-five percent of the experimental data was used for training, and 25% was used for testing. Individual neural networks were derived for each performance parameter. The results are shown in Table 28. The network structure and learning parameters were optimized to obtain high accuracy with minimal training. The prediction errors of the models were less than 6.5%.

Table 28. Neural Network Parameters for VCO

Output Parameter	**NN Structure**	**η**	**Prediction Error**	
			RMSE	**%RMSE**
Tuning Range	4-5-1	0.01	0.14	6.5
Phase Noise	4-8-1	0.01	1.15	1.8
Output Power	4-11-1	0.01	5.14	4.0

6.4.3. Design Centering

Neuro-genetic design centering was performed on the mean values of the VCO design parameters, and the standard deviations were assumed to be constant and independent of means. The acceptable specification limits for the tuning range, phase noise and output power were defined as:

$$\begin{aligned} &2.15\ GHz \le Tuning\ \text{R}ange \le 2.75\ GHz \\ &Phase\ Noise \le -92.5\ \text{dBc/Hz} \\ &Output\ Power \ge 55\ \mu W \end{aligned} \tag{22}$$

For an oscillator design, a higher value of tuning range and output power is desired, but a low value phase noise is required. Neuro-genetic design centering results in an increase of yield from 8% to 85% in just 24 iterations (Figure 48). The results of design centering for the VCO are summarized in Table 29

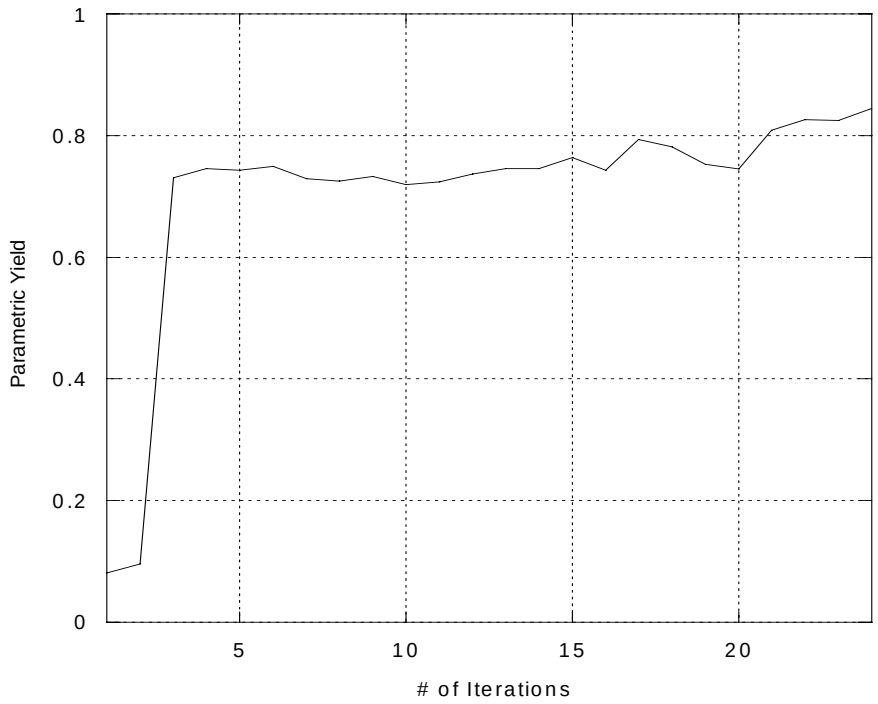


Figure 48. Parametric yield of VCO vs. # of iterations.

Table 29. VCO Design Centering

	Initial Value (Yield=8%)		**Final Value (Yield=85%)**	
Input Parameters	**Mean**	**Std**	**Mean**	**Std**
Emitter Length	4.03	0.4	4.08	0.4
Ibias	6.63	0.4	7.63	0.4
Cvardim	22.02	1	24.84	1
$L_{package}$	65.65	2.5	66.23	2.5
Output Parameters	**Mean**	**Std**	**Mean**	**Std**
Tuning Range	2.06	0.075	2.23	0.074
Phase Noise	-93.58	0.284	-93.63	0.006
Output Power	56.12	1.139	56.47	0.955

6.4.4. Yield Sensitivity Histograms

The results of design centering for the VCO are illustrated using yield sensitivity histograms. Figures 49 and 50 show a comparison of tuning range before and after design centering, respectively. As shown in Figure 49, a large proportion of the devices have tuning range below 2.15 GHz before design centering, resulting in low parametric yield. However, after design centering (Figure 50), parametric yield is improved substantially. Similar results can be observed from the histogram of output power (Figures 51-52).

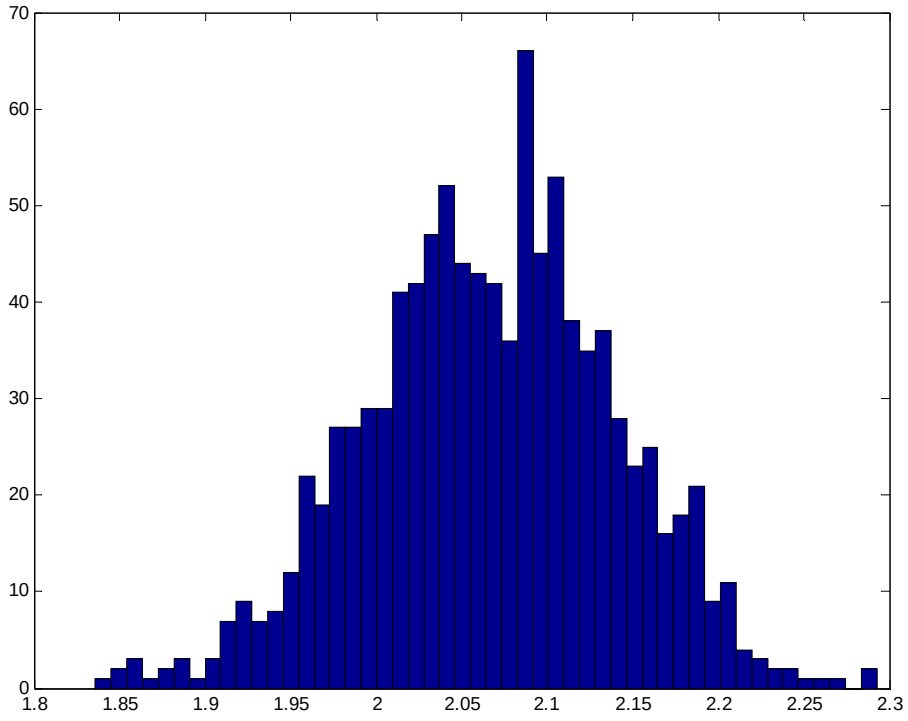


Figure 49. Yield histogram of tuning range before design centering

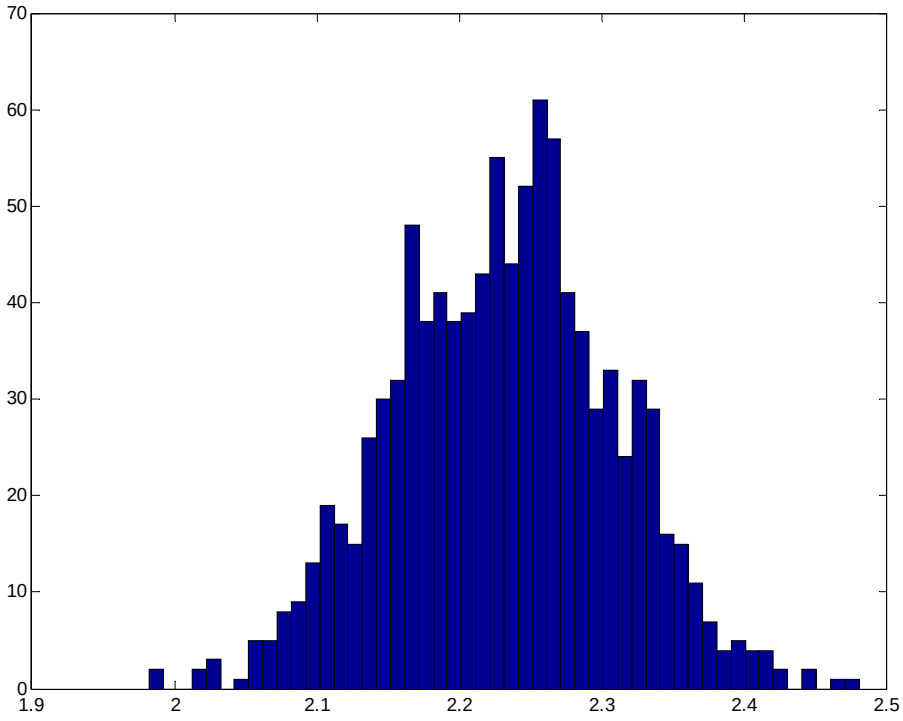


Figure 50. Yield histogram of tuning range after design centering

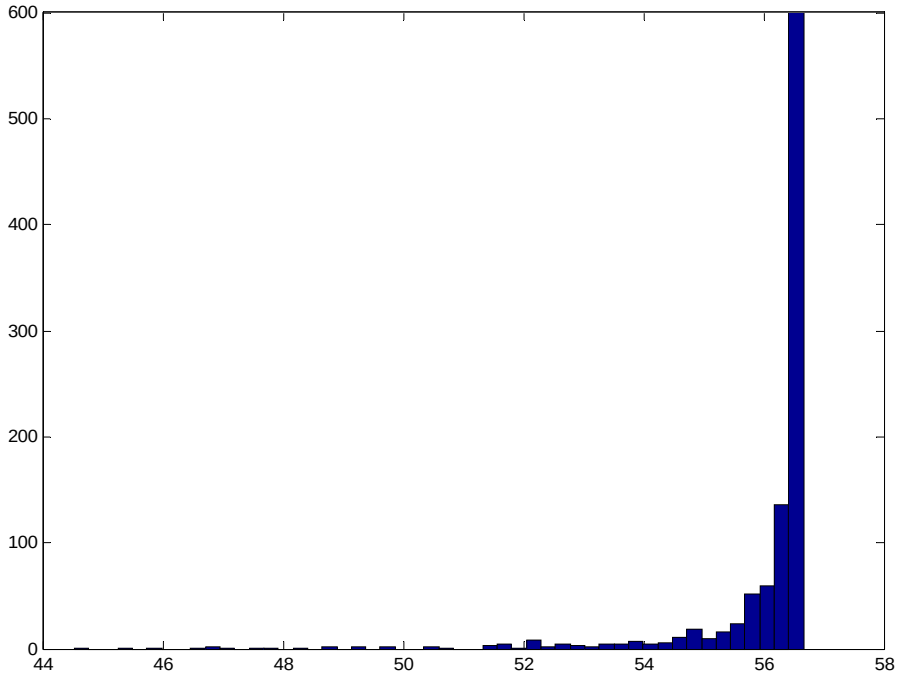


Figure 51. Yield histogram of output power before design centering

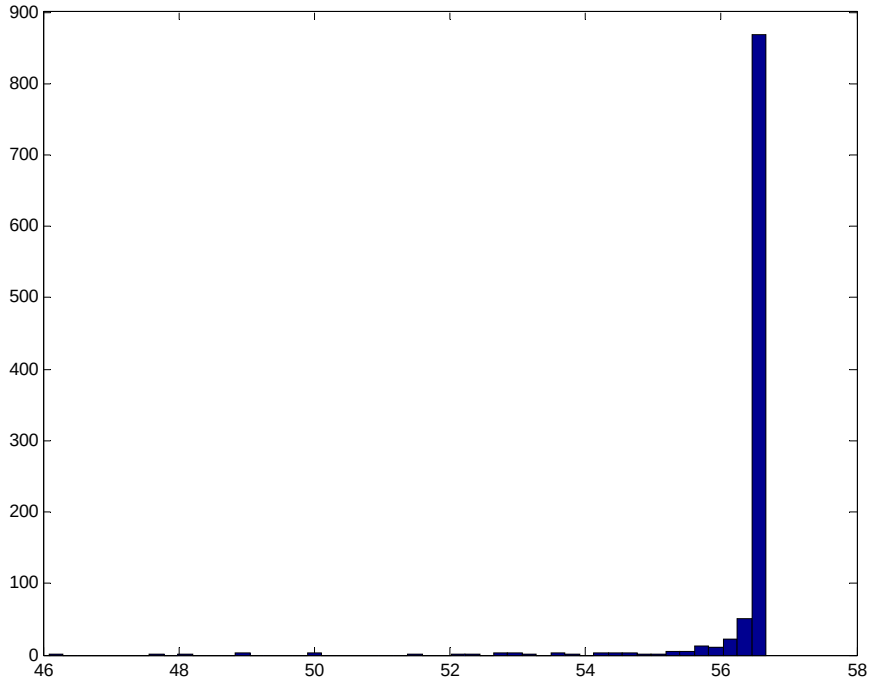


Figure 52. Yield histogram of output power after design centering

6.5 VCO Design Centering with non normal distribution

The distribution of input parameters for the initial examples using the SiGe HBT and VCO were normal, and the electrical performance specifications were also normal, except for the output power of the VCO. The design centering problem with normal input and output distributions is actually soluble using geometrical and hill climbing methods, since there is a linear functional relationship between input and output distributions. However, yield optimization problems with non-normal distributions are nonlinear optimization problems, and traditional methods are insufficient in such cases.

To illustrate the effectiveness of the proposed neuro-genetic method, design centering was performed again on the mean values of the VCO design parameters, and the standard

deviations were assumed to be constant and independent of means. However, the distribution of bias currents and package inductances were chosen to be uniform random, with a standard deviation of 10% of the range of variation in means. The emitter length and varactor dimensions were chosen to have normal distributions, with standard deviations of 5% of the range of variation of means. Table 30 summarizes the range of means, distribution type, and standard deviation of input design variables. The acceptable specification limits for the tuning range, phase noise and output power were the same as specified in Equation (22).

Table 30. VCO Input Parameters with Normal and Non Normal Distributions

Input Parameter	**Range for Mean**		**Distribution type**	**Standard Deviation**
	Low	**High**		
Emitter Length (μm)	2	10	Normal	0.4
Ibias (mA)	2	10	Uniform Random	0.8
Cvardim (μm)	10	30	Normal	1
$L_{package}$ (pH)	50	100	Uniform random	5

Neuro-genetic design centering results in a yield increase from 0.01% to 71% in just 38 iterations (Figure 53). The results of design centering for the VCO are summarized in Table 31. The results of design centering for the VCO are also illustrated using yield sensitivity histograms. Figures 54 and 55 show a comparison of tuning range before and after design centering, respectively. As shown in Figure 54, a large proportion of the devices have tuning range below 2.15 GHz before design centering, resulting in low parametric yield. However, after design centering (Figure 55), parametric yield is improved substantially. Although the histogram of output power indicates that partial parametric yield decreases slightly, the significant yield improvement in tuning range

compensates for the fall due to output power, and hence, the overall yield increases (Figures 56-57). The proposed method is thus effective in yield enhancement for devices with non-normal input distributions.

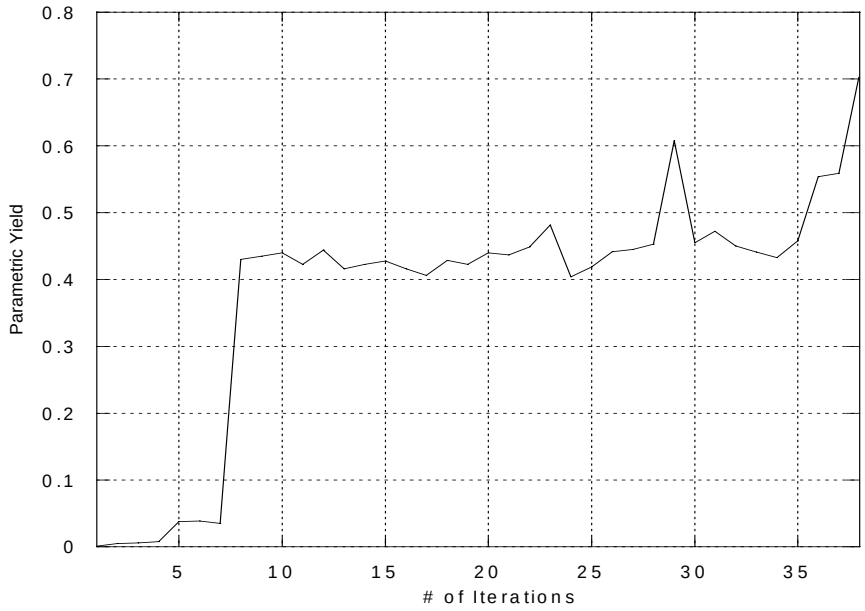


Figure 53. Yield of VCO vs. # of iterations with some non normal input variables.

Table 31. VCO Design Centering with Normal and Non Normal Distributions

	Initial Value (Yield=0.01%)		**Final Value (Yield=71%)**	
Input Parameters	**Mean**	**Std**	**Mean**	**Std**
Emitter Length	5.22	0.4	4.14	0.4
Ibias	5.86	0.8	7.99	0.8
Cvardim	21.69	1	24.91	1
$L_{package}$	68.12	5	60.59	5
Output Parameters	**Mean**	**Std**	**Mean**	**Std**
Tuning Range	1.92	0.068	2.27	0.106
Phase Noise	-92.58	0.912	-93.63	0.00001
Output Power	56.64	0.218	54.94	3.885

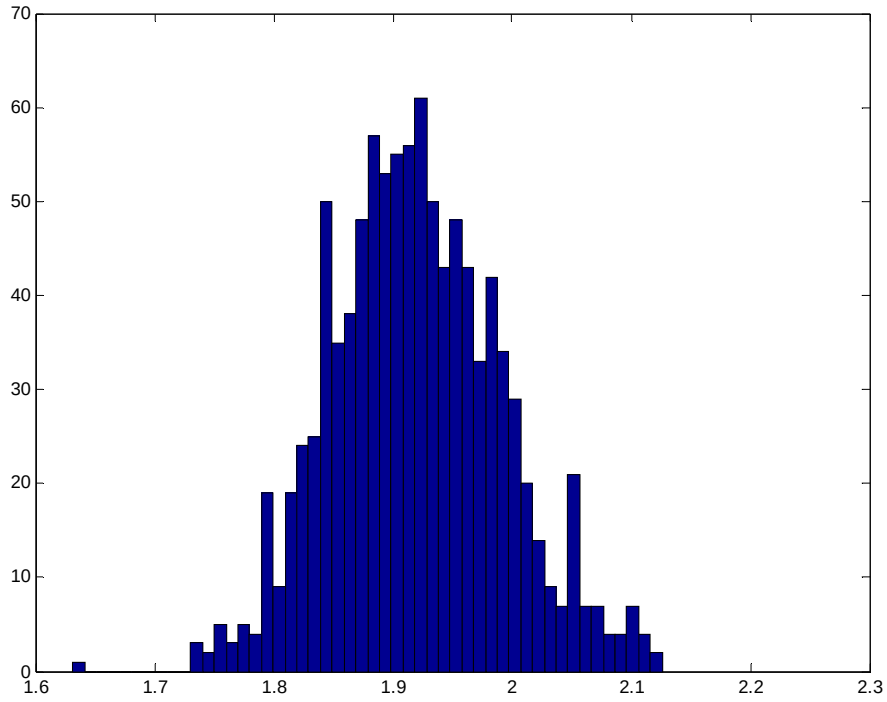


Figure 54. Yield histogram of tuning range before design centering for non normal case.

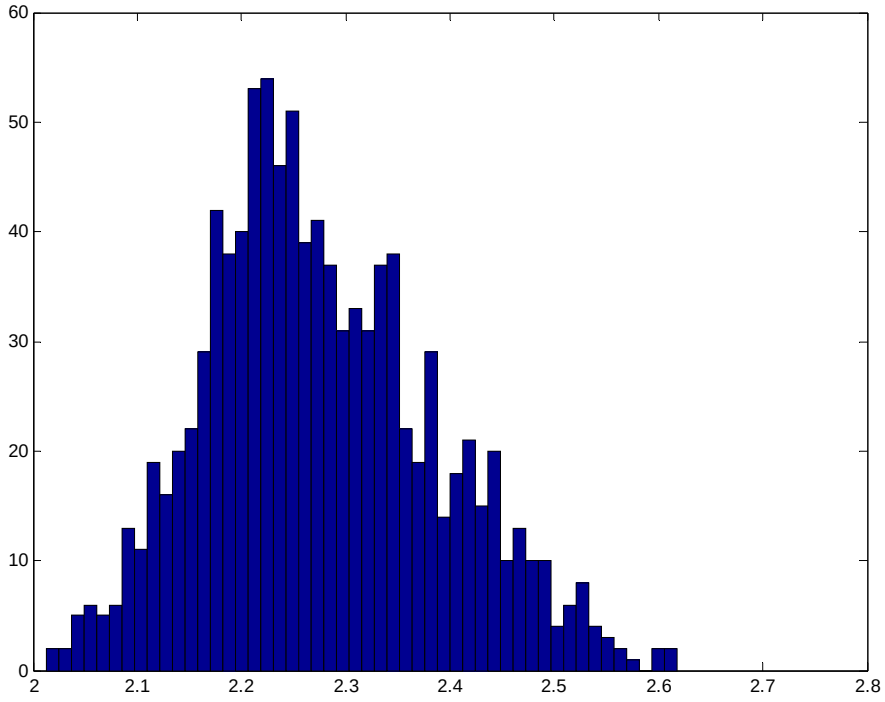


Figure 55. Yield histogram of tuning range after design centering for non normal case.

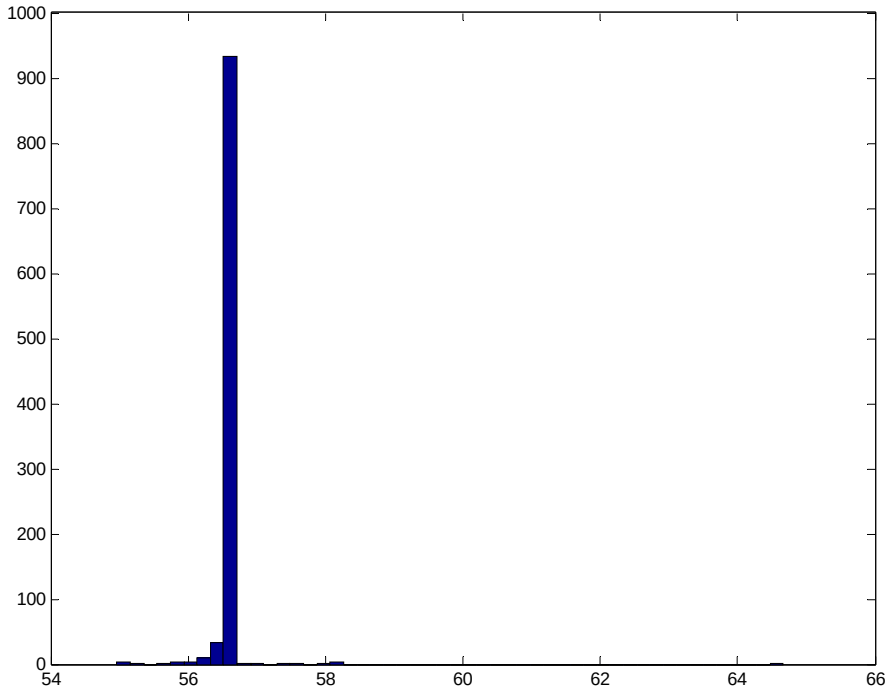


Figure 56. Yield histogram of output power before design centering non normal case.

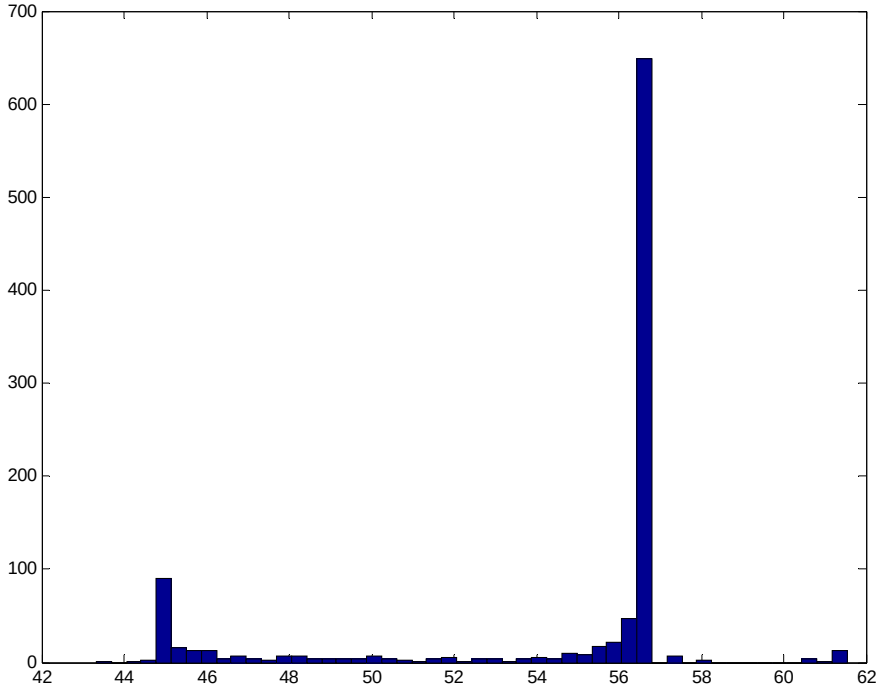


Figure 57. Yield histogram of output power after design centering for non normal case.

6.6 Summary

A neural network and genetic algorithm based design methodology has been developed and used for design centering of SiGe heterojunction bipolar transistors and 30GHz voltage- controlled oscillators. The proposed method results in yield enhancement of SiGe HBT from 25% to 75% in over 115 iterations. It requires only 24 iterations for to increase the yield of VCO from 8% to 85%. This method results in significant yield enhancement even for the case where the input variables have non normal distributions. Thus the proposed method is effective in yield enhancement and design centering microwave devices. Neuro-genetic design centering has the capability to handle large number of design variables. The neural network model does not require any assumptions about the system behavior, so it can be used to develop complex microwave component models involving device, circuit, package, and board or system level parameters. Thus, this method can be used for circuit, package, and systems level co-design, in which all the design parameters can be optimized simultaneously. This results in high yield for microwave devices since all the parameters are accounted for and optimized in pre-layout design stage.

CHAPTER 7

Conclusions and Future Work

In this thesis, tools and methodologies for modeling, analysis and design or synthesis have been presented. The tools and methodologies have been validated for several devices, circuits, and systems. This chapter discusses the contribution of this thesis for microwave design and suggests possible extensions and future work.

7.1 Contributions of the Research

This research strives to supplement the existing CAD tools by improving their accuracy and minimizing computational time. The methods developed can be implemented as tool box in existing CAD tools to enhance their performance for microwave design. This research presents a holistic approach for microwave circuit and systems design by providing modeling, analysis, and optimization or synthesis capability. It even strives to enhance yield of the microwave circuits for their economical commercial production. It also suggests a method for circuit package and system level co-design methodology for design of modern microwave systems with large number of correlated and interacting parameters. The methods that have evolved from this research have been used for validation of flip chip interconnects, multilayer inductors, multilayer capacitors, mm wave low pass filters, bandpass filters, SiGe heterojunction transistors, and mm wave voltage controlled oscillators. The generic nature of the tools suggests their possible extension for design of other microwave circuits as well. The proposed method

and tools can be indispensable to microwave designers for obtaining precise layout or process variables to meet targeted electrical specifications.

7.1.1. Neuro-Genetic Design and Synthesis

The first method developed herein was neuro-genetic design and synthesis. This is a holistic method, as it not only is used for modeling but for subsequent analysis, synthesis and optimization. The neural network is used for modeling, and genetic algorithms are used for subsequent optimization and synthesis. Neural network modeling is superior in accuracy to statistical methods and easier to derive than physical or analytical methods. It also has a significant speed advantage over electromagnetic simulators. It does not require any assumptions regarding the component or system behavior. The genetic algorithm approach is capable of efficient search through large nonlinear design space to obtain optimal value requiring only objective function value information. No derivative information or continuity of solution space assumptions is required. The method can also account for design tradeoffs using a weighted priority scheme. These features provide an advantage for this method over existing methods for microwave design in terms of speed, accuracy, and versatility. This method can be used in pre-fabrication and post fabrication stage.

7.1.2. Neuro-Genetic Design Centering

This research also developed a neuro-genetic design centering methodology for yield enhancement and design centering of microwave devices and circuits prior to high-volume manufacturing. This is the first application of neural networks and genetic

algorithms for yield optimization. Fast and accurate neural network models are used for yield calculation, providing greater accuracy than regression or statistical methods. The genetic approach is suitable for optimization of ill-behaved yield functions, since no derivative information is required, and it can search efficiently through a large space. This gives the proposed method significant advantage over gradient descent methods.

7.2 Conclusions and Summary

The neuro-genetic design method was used for modeling and analysis of flip chip interconnects with about 95% accuracy. The method was also used for synthesis of inductors and capacitors at 1.9 GHz and 2.4 GHz with precise electrical specifications. The method yielded layout values in close agreement (about 95%) with actual measured values. The neuro-genetic mm wave low pass filter synthesis resulted in synthesis of filters with desired insertion loss characteristics at 40 and 60 GHz. The results of modeling and synthesis of passive devices are summarized in Table 32. The novel priority scheme of the proposed methodology determined suitable layout values for wireless LAN bandpass filters accounting for tradeoffs among various targeted specifications. It also resulted in significant computational reduction in filter design.

Table 32. Summary of neuro-genetic design and synthesis

Type of Device	**Modeling Accuracy**	**Synthesis Accuracy**
1. Flip Chip Interconnects	6.7%	-
2. Multilayer Capacitor	5.6%	9%
3. Multilayer Inductor	3.6%	1.26%
4. Mm-wave Low Pass Filter	4.35%	2.2%
5. Bandpass Filters	1.98%	3.6%

Neuro-genetic design centering has been used for design centering of SiGe heterojuction transistors. It resulted in yield enhancement from 25% to 75% after 115 iterations. Neuro-genetic design centering results in an increase of yield from 8% to 85% in just 24 iterations for the 30 GHz voltage-controlled oscillator for input parameters with normal distributions and from 0.01% to 71% for non normal distributions. The results are summarized in Table 33. Thus, both the proposed methods were effective in microwave design, and the generic nature of the method suggests their possible use for design and optimization of microwave circuits and systems.

Table 33. Summary of neuro-genetic design centering

Type of Device	Modeling Accuracy	Yield Increase	# of Iterations
1. SiGe HBT	2.27%	25% to 75%	115
2. Mm-wave VCO	4.1%	8% to 85%	24
3. Mm-wave VCO (non normal)	4.1%	0.01% to 71%	38

7.3 Future Work

Further modification and enhancements to the proposed methods could occur at both stages i.e., the neural network modeling stage and genetic algorithm stage. At the neural network stage, apart from feed forward networks, other networks like recurrent networks can be incorporated to model time-dependent microwave circuits. The tool could incorporate a list of neural networks for the designer to select according to the application. The genetic algorithm performs very well during the initial stage of search but it slows significantly as it reaches closer to the optimal point. Therefore, the genetic algorithm can be used as a starting point and hill climbing approaches like gradient decent can be used to complete the optimization process. This could speed up the performance of genetic optimization.

APPENDIX A

ISE TCAD Program for SiGe HBT Simulation

TCAD Program for the Structure and Doping Profile of SiGe HBT

```
; Reinitializing DEVISE
(ise:clear)

; Creating polygonal  regions
(isegeo:create-polygon
 (list  (position -0.45 0.6 0.0)
        (position  1.2 0.6 0.0)
        (position  1.2 0.3 0.0)
        (position  1.095 0.3 0.0)
        (position  1.005 0.0 0.0)
        (position  0.795 0.0 0.0)
        (position  0.705 0.3 0.0)
        (position  0.315 0.3 0.0)
        (position  0.225 0.0 0.0)
        (position -0.225 0.0 0.0)
        (position -0.315 0.3 0.0)
        (position -0.45 0.3 0.0)
        (position -0.45 0.6 0.0) )
 "SiliconGermanium" "Substate")
; Creating rectangular regions
(isegeo:create-rectangle
  (position -0.225 -0.075 0.0) (position  0.225  0.0 0.0)
"SiliconGermanium" "SiGeBase")
(isegeo:create-rectangle
  (position -0.6 -0.075 0.0) (position -0.15 -0.15 0.0) "PolySilicon"
"Baseleft")
(isegeo:create-rectangle
  (position  0.15 -0.075 0.0) (position  0.45 -0.15 0.0) "PolySilicon"
"Baseright")
(isegeo:create-rectangle
  (position -0.075 -0.075 0.0) (position  0.075 -0.3 0.0) "PolySilicon"
"Emitter")
(isegeo:create-rectangle
  (position  0.825  0.0 0.0) (position  0.975 -0.3 0.0) "Aluminium"
"CollectorCont")
(isegeo:create-rectangle
  (position -0.6 -0.15 0.0) (position -0.45 -0.3 0.0) "Aluminium"
"BaseCont")

; Creating device insulation using overlap resolution
(isegeo:set-default-boolean "BAB")
(isegeo:create-rectangle
  (position -0.6 -0.3 0.0) (position  1.35 0.6 0.0) "SiO2"
"Insulation")

; Defining contacts
```

```
(isegeo:define-contact-set "base"      4.0 (color:rgb 1.0 0.0 0.0 )
"##" )
(isegeo:define-contact-set "emitter"   4.0 (color:rgb 0.0 1.0 0.0 )
"##" )
(isegeo:define-contact-set "collector" 4.0 (color:rgb 0.0 0.0 1.0 )
"##" )

(isegeo:set-current-contact-set "base")
(isegeo:set-contact-boundary-edges (find-body-id (position -0.525 -
0.225 0.0)) "base")
(isegeo:delete-region (find-body-id (position -0.525 -0.225 0.0)))

(isegeo:set-current-contact-set "collector")
(isegeo:set-contact-boundary-edges (find-body-id (position 0.9 -0.15
0.0)))
(isegeo:delete-region (find-body-id (position 0.9 -0.15 0.0)))

(isegeo:set-current-contact-set "emitter")
(isegeo:define-2d-contact (find-edge-id (position 0.0 -0.3 0.0))
"emitter")

; Refinement Boxes

(isedr:define-refinement-window "BulkN" "Rectangle"  (position -0.65 -
0.2 0.000000)  (position 1.4 0.6 0.000000) )

(isedr:define-refinement-window "PolysTop" "Rectangle"  (position -0.65
-0.16 0.000000)  (position 0.50 -0.05 0.000000) )

(isedr:define-refinement-window "CollectorRight" "Line"  (position 0.45
-0.075 0.000000)  (position 1.20 -0.075 0.000000) )

(isedr:define-refinement-window "Base" "Line"  (position -0.225 -0.075
0.000000)  (position 0.225 -0.075 0.000000) )

(isedr:define-refinement-window "CollectorLeft" "Line"  (position -0.45
-0.015 0.000000)  (position 0.45 -0.015 0.000000) )

; Doping Windows
; Doping Definitions
; Doping Placements

(isedr:define-constant-profile "lowN" "ArsenicActiveConcentration"
1.50e17)

(isedr:define-constant-profile-placement "baseColl" "lowN" "BulkN")

(isedr:define-constant-profile "hiP" "BoronActiveConcentration"
9.20e+19)

(isedr:define-constant-profile-region "polyLeftP+" "hiP" "Baseleft")

(isedr:define-constant-profile-region "polyRightP+" "hiP" "Baseright")


(isedr:define-constant-profile "N10e19" "ArsenicActiveConcentration"
1.00e+20)
```

```
(isedr:define-constant-profile-region "poly_emitter" "N10e19"
"Emitter")


(isedr:define-analytical-profile-placement "collectorNR" "Nplus2.0e19"
"CollectorRight" "NoSymm" "NoReplace" "Eval")

(isedr:define-gaussian-profile "Nplus2.0e19"
"ArsenicActiveConcentration" "PeakPos" 0.0  "PeakVal" 1.0e19
"ValueAtDepth" 5.00e17 "Depth" 0.400 "Gauss"  "Factor" 0.001)

(isedr:define-refinement-window "Base" "Line"  (position -0.225 -0.075
0.000000)  (position 0.225 -0.075 0.000000) )

(isedr:define-analytical-profile-placement "collectorNL" "Nplus1.0e18"
"CollectorLeft" "NoSymm" "NoReplace" "Eval")

(isedr:define-gaussian-profile "Nplus1.0e18"
"ArsenicActiveConcentration" "PeakPos" 0.0  "PeakVal" 1.0e17
"ValueAtDepth" 1.00e16 "Depth" 0.040 "Gauss"  "Factor" 0.001)

(isedr:define-refinement-window "Base" "Line"  (position -0.225 -0.075
0.000000)  (position 0.225 -0.075 0.000000) )

(isedr:define-analytical-profile-placement "baseP" "Pplus5.00e19"
"Base" "NoSymm" "NoReplace" "Eval")

(isedr:define-gaussian-profile "Pplus5.00e19"
"BoronActiveConcentration" "PeakPos" 0.0  "PeakVal" 5.00e19
"ValueAtDepth" 1.00e19 "Depth" 0.025 "Gauss"  "Factor" 0.001)

(isedr:define-refinement-window "EmitterDiffusion" "Line"  (position -
0.09 -0.075 0.000000)  (position 0.09 -0.075 0.000000) )

(isedr:define-analytical-profile-placement "EmitterDiffN"
"Nplus1.00e20" "EmitterDiffusion" "NoSymm" "NoReplace" "Eval")

(isedr:define-gaussian-profile "Nplus1.00e20"
"ArsenicActiveConcentration" "PeakPos" 0.0  "PeakVal" 1.00e20
"ValueAtDepth" 1.00e19 "Depth" 0.030 "Gauss"  "Factor" 0.010)

(isedr:define-refinement-window "BuriedCollector" "Line"  (position -
0.50  0.400 0.000000)  (position 1.25  0.400 0.000000) )

(isedr:define-analytical-profile-placement "BuriedCollN" "N1.00e18"
"BuriedCollector" "Symm" "NoReplace" "Eval")

(isedr:define-gaussian-profile "N1.00e18" "ArsenicActiveConcentration"
"PeakPos" 0.0  "PeakVal" 1.00e18 "ValueAtDepth" 5.00e17 "Depth" 0.100
"Gauss"  "Factor" 0.050)

(isedr:define-refinement-window "BaseEmitterP" "Line"  (position -
0.2250  -0.045 0.000000)  (position 0.225  -0.045 0.000000) )

(isedr:define-analytical-profile-placement "BaseEmitterDiffP"
"P5.00e18" "BaseEmitterP" "Symm" "NoReplace" "Eval")
```

```
(isedr:define-gaussian-profile "P5.00e18" "BoronActiveConcentration"
"PeakPos" 0.0  "PeakVal" 7.50e18 "ValueAtDepth" 5.00e17 "Depth" 0.020
"Gauss"  "Factor" 0.010)

; Refinement Boxes

(isedr:define-refinement-window "GlobalRefinement" "Rectangle"
(position -0.65 -0.4 0.000000)  (position 1.45 0.7 0.000000) )

(isedr:define-refinement-window "PolysTop" "Rectangle"  (position -0.65
-0.16 0.000000)  (position 0.50 -0.05 0.000000) )

(isedr:define-refinement-window "base_refine" "Rectangle"  (position -
0.250000 -0.100000 0.000000)  (position 0.250000 0.0250000 0.000000) )

(isedr:define-refinement-window "collector_refineL" "Rectangle"
(position -0.350000 0.025000 0.000000)  (position 0.450000 0.4000000
0.000000) )

(isedr:define-refinement-window "collector_refineR" "Rectangle"
(position  0.500000 0.925000 0.000000)  (position 1.150000 0.4200000
0.000000) )

(isedr:define-refinement-window "base_emitterJn" "Rectangle"  (position
-0.080000 -0.080000 0.000000)  (position 0.080000 -0.0250000 0.000000)
)

; Doping Windows
; Doping Definitions
; Doping Placements

(isedr:define-refinement-size "DefaultCourse" 0.1 0.08 0.05 0.02 )

(isedr:define-refinement-placement "default" "DefaultCourse"
"GlobalRefinement" )

(isedr:define-refinement-function "DefaultCourse" "DopingConcentration"
"MaxTransDiff" 1.0)

(isedr:define-refinement-size "DefaultCourse1" 0.04 0.02 0.005 0.005 )

(isedr:define-refinement-placement "top" "DefaultCourse1" "PolysTop" )

(isedr:define-refinement-function "DefaultCourse1"
"DopingConcentration" "MaxTransDiff" 1.000000)

(isedr:define-refinement-size "Base1" 0.08 0.010 0.020 0.002 )

(isedr:define-refinement-placement "BasePlace" "Base1" "base_refine" )

(isedr:define-refinement-function "Base1" "DopingConcentration"
"MaxTransDiff" 1.0)

(isedr:define-refinement-size "Collector1" 0.08 0.040 0.040 0.01 )
```

```
(isedr:define-refinement-placement "CollectorPlaceL" "Collector1"
"collector_refineL" )

(isedr:define-refinement-placement "CollectorPlaceR" "Collector1"
"collector_refineR" )

(isedr:define-refinement-function "Collector1" "DopingConcentration"
"MaxTransDiff" 0.5)

(isedr:define-refinement-size "JunctionRefine" 0.01 0.0025 0.001
0.00025 )

(isedr:define-refinement-placement "BEJn" "JunctionRefine"
"base_emitterJn" )

(isedr:define-refinement-function "JunctionRefine"
"DopingConcentration" "MaxTransDiff" 1.000000)

; Saving the model
(iseio:save-dfise-bnd (part:entities (filter:type "solid?"))
"@boundary/o@")
(isedr:write-cmd-file "@commands/o@")
```

Material properties and coefficients for SiGe HBT

```
Material = "SiliconGermanium" {
Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma
  * tau(T) = tau * ( (T/300)^Talpha )          (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
        taumin  = 0.0000e+00 ,  0.0000e+00      # [s]
        taumax  = 1.0000e-05 ,  3.0000e-06      # [s]
        Nref    = 1.0000e+16 ,  1.0000e+16      # [cm^(-3)]
        gamma   = 1 ,   1       # [1]
        Talpha  = -1.5000e+00 , -1.5000e+00     # [1]
        Tcoeff  = 2.55 ,        2.55    # [1]
        Etrap   = 0.0000e+00    # [eV]
}

Auger * coefficients:
{ * R_Auger = ( C_n n + C_p p ) ( n p - ni_eff^2)
  * with C_n,p = (A + B (T/T0) + C (T/T0)^2) (1 + H exp(-{n,p}/N0))
        A       = 6.7000e-32 ,  7.2000e-32      # [cm^6/s]
        B       = 2.4500e-31 ,  4.5000e-33      # [cm^6/s]
        C       = -2.2000e-32 , 2.6300e-32      # [cm^6/s]
        H       = 3.46667 ,     8.25688 # [1]
        N0      = 1.0000e+18 ,  1.0000e+18      # [cm^(-3)]
}
DopingDependence:
{
  * For doping dependent mobility model three formulas
  * can be used. Formula1 is based on Masetti et al. approximation.
  * Formula2 uses approximation, suggested by Arora.
        formula = 1 ,   1       # [1]
  * If formula=1, model suggested by Masetti et al. is used:
```

```
  * mu_dop = mumin1 exp(-Pc/N) + (mu_const - mumin2)/(1+(N/Cr)^alpha)
  *                            - mu1/(1+(Cs/N)^beta)
  * with mu_const from ConstantMobility
       mumin1  = 52.2 ,        44.9    # [cm^2/Vs]
       mumin2  = 52.2 ,        0.0000e+00      # [cm^2/Vs]
       mu1     = 43.4 ,        29      # [cm^2/Vs]
       Pc      = 0.0000e+00 ,  9.2300e+16      # [cm^3]
       Cr      = 9.6800e+16 ,  2.2300e+17      # [cm^3]
       Cs      = 3.4300e+20 ,  6.1000e+20      # [cm^3]
       alpha   = 0.68 ,        0.719   # [1]
       beta    = 2 ,   2       # [1]
}
```

APPENDIX B

MATLAB Code for Neuro-Genetic Design Centering

MATLAB Program for Voltage-Controlled Oscillator Design Centering

Program for Genetic Manipulation

```
##################genetic.m#########################
% This is main genetic function
function genetic
% Clear all
global N M FNET1 FNET2 FNET3
%%%###################Load the trained neural networks
% load NETtrain1;
% load NETtrain2;
%%%###################Assign the values to the parameters
N=10;                                % The size of population, has to be even.
PCross=0.65;                         % The probability of crossover
Pmutate=0.01;                        % Mutation Value
GeneNum=10000;                       % Max # of generations(iterations)
NumofInputs=4;                       % # of input parameters to the function
limits=[4, 8; 4, 8; 15, 25; 60, 90];  % range of input parameters
ChromLengths=[100, 100, 100, 100];    % The length of input chromosomes
M=sum(ChromLengths);                 % The length of chromosomes
ReproduceN=N/2;                      % # used during reproduction
target=0.9;                          % Targeted Yield
%%%#################Create initial random population
%Generate N population of length M using random function
Pop=round(rand(N,M));
%%%#################Start the iteration
for k=1:GeneNum
   %Decode the input population by using 'PopDecode' function
   AllXvalues=PopDecode(Pop,NumofInputs,ChromLengths,limits);
   % Determine the value of Y i.e. yield for the currect input population
   for m=1:N
     [yield(m),mu(m,:),ystd(m,:),yvar(m,:)] =
yieldfun(AllXvalues(m,:),FNET1,FNET2,FNET3);%yield(m)=
yieldfun(AllXvalues(m,:));
   end % m
   % Pick the best value of the sample and print it in a file
   [best,index]=max(yield);
   fid = fopen('output.data','a');
```

```
    fprintf(fid,'%g \t',k);
    fprintf(fid,'%g \t',AllXvalues(index,:));
    fprintf(fid,'%g \t', best);
    fprintf(fid,'%g \t', mu(index,:));
    fprintf(fid,'%g \t',ystd(index,:));
    fprintf(fid,'\n');
    status = fclose(fid);
    if best >= target
       break;
    end
    % Determine the fitness of each sample and add the fitness
    FitListSum=cumsum(yield);
    % Perform reproduction
    NewPop=zeros(N,M);
     for j=1:ReproduceN
          % select two samples using roulett wheel approach
          index=zeros(1,2);
          for r=1:2
          randomOne=rand(1)*FitListSum(N);
          temp=FitListSum'-randomOne*ones(N,1);
          index(r)=min(find(temp>=0));
          end %r
        ParentIndices=index;
        Parents=Pop(ParentIndices,:);
        Xvalues=PopDecode(Parents,NumofInputs,ChromLengths,limits);
          [a,b]=size(Xvalues);
          for s=1:a
          ParentFitness(s,:)=yieldfun(Xvalues(s,:));
          end %s
        % Crossover: Sharing of genes during reproduction
         Child2=zeros(2,M);
         BeforeMu=crossover(PCross,Parents); %2xM Matrix
        % Perform Mutation
         Child2=mutate(Pmutate,BeforeMu,2);  %2xM Matrix
         NewPop(2*j-1:2*j,:)=Child2;
      end %j
    Pop=NewPop;
end % for k(GeneNum)

##################mutate.m#########################
% This is mutation function
function outy=mutate(Pmutate,chromosome,NofChromosome)
%function outy=mutate(PMutate,BeforeMu,NofChromosome)
%Each element of chromosome is called allel
%M : The length of chromosome
%Nof Chormosome(=2) : Normally two children
```

```
global N M
clear outy
outy=chromosome;
%for all bits (in our case 10) of all vectors (in our case 2)
%inverse from 0 to 1 or from 1 to with probability pmutate
for k=1: NofChromosome
  for j=1:M
     if (rand(1)<Pmutate)==1
       outy(k,j)=xor(chromosome(k,j),1);
     end;
  end;%for j
end;%for k
```

##################crossover.m#########################

```
% This is crossover function
function children=crossover(Pcross,parents)
%Function children=crossover(pcross,parents)
%parents,children: 2xM
global N M
children=zeros(2,M);

if (rand(1)<Pcross)==1
  %True: select cross site at random [1 .. (M-)]
  crossAt=fix(rand(1)*(M-1))+1;
  children(1,:)=[parents(1,1:crossAt),parents(2,crossAt+1:M)];
  children(2,:)=[parents(2,1:crossAt),parents(1,crossAt+1:M)];
else
  children=parents;
end;
```

##################PopDecode.m#########################

```
% This is a function to decode the population
function  ybase10=PopDecode(chromosome,NumofInputs,ChromLengths,limits);
%Population decoder
[X,Y]=size(chromosome);
% [range]=minmax(Ranges);          %min and max values of input set
RangeVal=limits(:,2)-limits(:,1);
ybase10=zeros(X,NumofInputs);
ChrLenPt=1;                        %Chromosome pointer
for n=1:X
  clear ChrLenPt
  ChrLenPt=1;
  for k=1:NumofInputs
    j=(ChromLengths(k)-1):-1:0;
    series2=2.^j;
```

```
    ChrEnd=ChrLenPt:ChrLenPt+ChromLengths(k)-1;

ybase10(n,k)=chromosome(n,ChrEnd)*series2'*(RangeVal(k))/(2^ChromLengths(k))+li
mits(k,1);
    ChrLenPt=ChrLenPt+ChromLengths(k);
    clear j, series2;
  end%k
end%n
```

Program for Yield Calculation of VCO

```
##################yieldfun.m#########################
% This is Yield function
function [yield,mu,ystd,yvar] = yieldfun(means,FNET1,FNET2,FNET3)
load NETtrain1;
load NETtrain2;
load NETtrain3;
%%%################### Enter the values of Inputs, # of samples, limits
NumofInputs=4;    %# of Inputs
samples=1000;    %# of samples
stdev=[0.4, 0.4, 1, 2.5];   %Vector of standard deviation for each input parameters
type=[1, 1, 1, 1];    % Vector of type of distrubutiom : random =0, normal=1

%%%################## Enter the # of outputs and specification limits
outputs=3;    %# of outputs
goodlimit= [2.15, 2.75; -100, -92.5; 55, 100];    % Vector of minmax allowed output
parameters

%%%##################
for j=1:samples
   for i= 1:NumofInputs
      if type(i)== 0
      invector(j,i)= means(i)-(stdev(i)/2)+rand(1)*(stdev(i));
      else
      invector(j,i)=means(i)+ randn(1)*stdev(i);
      end
   end
end
% Call the neural networks for each output
%invector
[y1]=sim(FNET1,invector');
[y2]=sim(FNET2,invector');
[y3]=sim(FNET3,invector');
% Put the output values in the y vector
for u=1:samples
   y(u,1)=y1(u);
   y(u,2)=y2(u);
```

```
   y(u,3)=y3(u);
end

%%%%##########################################################################
#########
 % Plot histograms
 hist(y3,50);

%%%%##########################################################################
#########
% Find the Yield of the circuit.
mu=mean(y);ystd=std(y);yvar=var(y); % Find the mean standard deviation and mean of
the output
good=ones(1,samples);
for t=1:samples
   for n=1:outputs
      if ~((y(t,n)>=goodlimit(n,1)) && (y(t,n)<=goodlimit(n,2)))
         good(t)=0;
      end
   end
end
[crap holy]=size(find(good));
yield=holy/samples;
%%%##########################################################################
#####
% Calculate Cpk
% for r=1:outputs
%    clow=(mu(r)-limits(r,1))/(3*ystd(r));
%    chigh=(limits(r,2)-mu(r))/(3*ystd(r));
%    if clow<=chigh
%       cpk(r)=clow;
%    else
%       cpk(r)=chigh;
%    end
% end
%%%##########################################################################
#####
```

Program for Neural Network Modeling of VCO

```
##################ftrain1.m#########################
clear
% Training Data sets
INtrain1=[
7.2     3.7     24      83
7.4     2.7     27      92
3.1     4.5     19      50
```

```
3.6	4.3	16	52
6.2	8	23	55
5.1	6.3	18	73
6.8	2.2	13	89
8.3	5.6	28	96
5.3	2.9	17	79
5.8	4.1	26	85
2.7	7.1	27	94
8.6	9.1	12	92
3.4	3.4	14	100
4.8	7.9	30	70
9.5	3.1	20	64
4.6	10	28	98
7.9	8.4	11	88
2.1	5.8	10	54
2.9	5.4	14	61
4.4	3.8	25	78
4.1	8.8	23	60
8.1	8.6	29	66
6.7	9.5	18	75
2.4	6.7	15	56
5.5	7	16	68
9.5	4.8	25	63
6.3	2.3	22	87
7.6	9.7	21	81
9.8	5.2	20	58
9.2	6	13	75
8.7	7.3	21	70
3.7	7.7	12	84]';

OUTtrain1=[
1.94
2.1
1.97
1.74
1.99
1.72
1.26
2.1
1.58
2.08
2.57
1.18
1.6
2.42
1.69
```

```
2.35
1.12
1.35
1.63
2.23
2.1
2.21
1.66
1.83
1.57
2
1.92
1.83
1.69
1.25
1.79
1.42]';
%Neural Network structure formation
FNET1=newff([2.0 10.0; 2.00 10.0; 10.0 30.0; 50 100],[5 1],{'tansig' 'purelin'});
% Neural Network Training Parameters
  FNET1.trainParam.epochs= 100000;       %Maximum number of epochs to train
  FNET1.trainParam.goal= 0.001;         %Performance goal
  FNET1.trainParam.max_fail=5;         %Maximum validation failures
  FNET1.trainParam.mem_reduc=1;       %Factor to use for memory/speed trade off.
  FNET1.trainParam.min_grad=1e-30;     %Minimum performance gradient
  FNET1.trainParam.mu=10;            %Initial Mu
  FNET1.trainParam.mu_dec=0.01;        %Mu decrease factor
  FNET1.trainParam.mu_inc=100;         %Mu increase factor
  FNET1.trainParam.mu_max=1e30;        %Maximum Mu
  FNET1.trainParam.show=100;          %Epochs between displays (NaN for no displays)
[FNET1,tr1]=train(FNET1,INtrain1,OUTtrain1);
% End of training
% Save the work space
save('NETtrain1');
```

##################ftrain2.m#########################

```
clear
% Training Data sets
INtrain2=[
7.2     3.7     24      83
7.4     2.7     27      92
3.1     4.5     19      50
3.6     4.3     16      52
6.2     8       23      55
5.1     6.3     18      73
6.8     2.2     13      89
```

```
8.3	5.6	28	96
5.3	2.9	17	79
5.8	4.1	26	85
2.7	7.1	27	94
8.6	9.1	12	92
3.4	3.4	14	100
4.8	7.9	30	70
9.5	3.1	20	64
4.6	10	28	98
7.9	8.4	11	88
2.1	5.8	10	54
2.9	5.4	14	61
4.4	3.8	25	78
4.1	8.8	23	60
8.1	8.6	29	66
6.7	9.5	18	75
2.4	6.7	15	56
5.5	7	16	68
9.5	4.8	25	63
6.3	2.3	22	87
7.6	9.7	21	81
9.8	5.2	20	58
9.2	6	13	75
8.7	7.3	21	70
3.7	7.7	12	84]';

OUTtrain2=[
-92.2
-91.2
-93.5
-91.2
-93.9
-94
-93.2
-92.7
-94.6
-95
-93.4
-90.5
-90.8
-94.6
-90.6
-94
-91.1
-91.2
-92.3
```

```
-91.8
-93.4
-93
-92.9
-92.1
-93.8
-91.7
-94.8
-92.6
-91.1
-90.6
-91.9
-91.7]';
%Neural Network structure formation
FNET2=newff([2.0 10.0; 2.00 10.0; 10.0 30.0; 50 100],[8 1],{'tansig' 'purelin'});
% Neural Network Training Parameters
  FNET2.trainParam.epochs= 100000;       %Maximum number of epochs to train
  FNET2.trainParam.goal= 0.01;         %Performance goal
  FNET2.trainParam.max_fail=5;         %Maximum validation failures
  FNET2.trainParam.mem_reduc=1;        %Factor to use for memory/speed trade off.
  FNET2.trainParam.min_grad=1e-20;     %Minimum performance gradient
  FNET2.trainParam.mu=0.001;           %Initial Mu
  FNET2.trainParam.mu_dec=0.05;        %Mu decrease factor
  FNET2.trainParam.mu_inc=5;         %Mu increase factor
  FNET2.trainParam.mu_max=1e20;        %Maximum Mu
  FNET2.trainParam.show=100;           %Epochs between displays (NaN for no displays)
[FNET2,tr2]=train(FNET2,INtrain2,OUTtrain2);
% End of training
% Save the work space
save('NETtrain2');
```

##################ftrain3.m#########################

```
clear
% Training Data sets
INtrain2=[
7.2     3.7     24      83
7.4     2.7     27      92
3.1     4.5     19      50
3.6     4.3     16      52
6.2     8       23      55
5.1     6.3     18      73
6.8     2.2     13      89
8.3     5.6     28      96
5.3     2.9     17      79
5.8     4.1     26      85
2.7     7.1     27      94
```

```
8.6     9.1     12      92
3.4     3.4     14      100
4.8     7.9     30      70
9.5     3.1     20      64
4.6     10      28      98
7.9     8.4     11      88
2.1     5.8     10      54
2.9     5.4     14      61
4.4     3.8     25      78
4.1     8.8     23      60
8.1     8.6     29      66
6.7     9.5     18      75
2.4     6.7     15      56
5.5     7       16      68
9.5     4.8     25      63
6.3     2.3     22      87
7.6     9.7     21      81
9.8     5.2     20      58
9.2     6       13      75
8.7     7.3     21      70
3.7     7.7     12      84]';

OUTtrain2=[
-92.2
-91.2
-93.5
-91.2
-93.9
-94
-93.2
-92.7
-94.6
-95
-93.4
-90.5
-90.8
-94.6
-90.6
-94
-91.1
-91.2
-92.3
-91.8
-93.4
-93
-92.9
```

```
-92.1
-93.8
-91.7
-94.8
-92.6
-91.1
-90.6
-91.9
-91.7]';
%Neural Network structure formation
FNET2=newff([2.0 10.0; 2.00 10.0; 10.0 30.0; 50 100],[8 1],{'tansig' 'purelin'});
% Neural Network Training Parameters
  FNET2.trainParam.epochs= 100000;       %Maximum number of epochs to train
  FNET2.trainParam.goal= 0.01;         %Performance goal
  FNET2.trainParam.max_fail=5;         %Maximum validation failures
  FNET2.trainParam.mem_reduc=1;        %Factor to use for memory/speed trade off.
  FNET2.trainParam.min_grad=1e-20;     %Minimum performance gradient
  FNET2.trainParam.mu=0.001;           %Initial Mu
  FNET2.trainParam.mu_dec=0.05;        %Mu decrease factor
  FNET2.trainParam.mu_inc=5;           %Mu increase factor
  FNET2.trainParam.mu_max=1e20;        %Maximum Mu
  FNET2.trainParam.show=100;           %Epochs between displays (NaN for no displays)
[FNET2,tr2]=train(FNET2,INtrain2,OUTtrain2);
% End of training
% Save the work space
save('NETtrain2');
```

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PUBLICATIONS

Journal and Magazine Publications

[1] **R. J. Pratap**, D. Staiculescu, S. Pinel, J. Laskar, and G. S. May, "Modeling and sensitivity analysis of circuit parameters for flip-chip interconnects using neural networks," *IEEE Transactions on Advanced Packaging*, vol. 28, pp. 71-78, Feb. 2005.

[2] **R. J. Pratap**, S. Sarkar, S. Pinel, J. Laskar, and G. S. May, "Neuro-genetic microwave design," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

[3] **R. J. Pratap**, P. Sen, C. Davis, G. S. May, and J. Laskar, "Neuro-genetic design centering for design for manufacturability," submitted to *IEEE Transactions on Semiconductor Manufacturing*.

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Conference Publications

[5] **R. J. Pratap**, J.H. Lee, S. Pinel, G.S. May, J. Laskar, and M.M. Tentzeris, "Millimeter wave RF front end design using neuro-genetic algorithms," in Proc. *2005 Electronic Components and Technology Conference*, vol.1, pp. 1802-1806, June 2005.

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His research interests include development of artificial intelligence based tools for modeling, analysis and optimization of microwave circuits. His research interests also involve signal integrity, package development, transmission line analysis and multilayer inductor, capacitor and passive filter design. He is also interested in design centering and design for manufacturability in microwave circuits and systems.